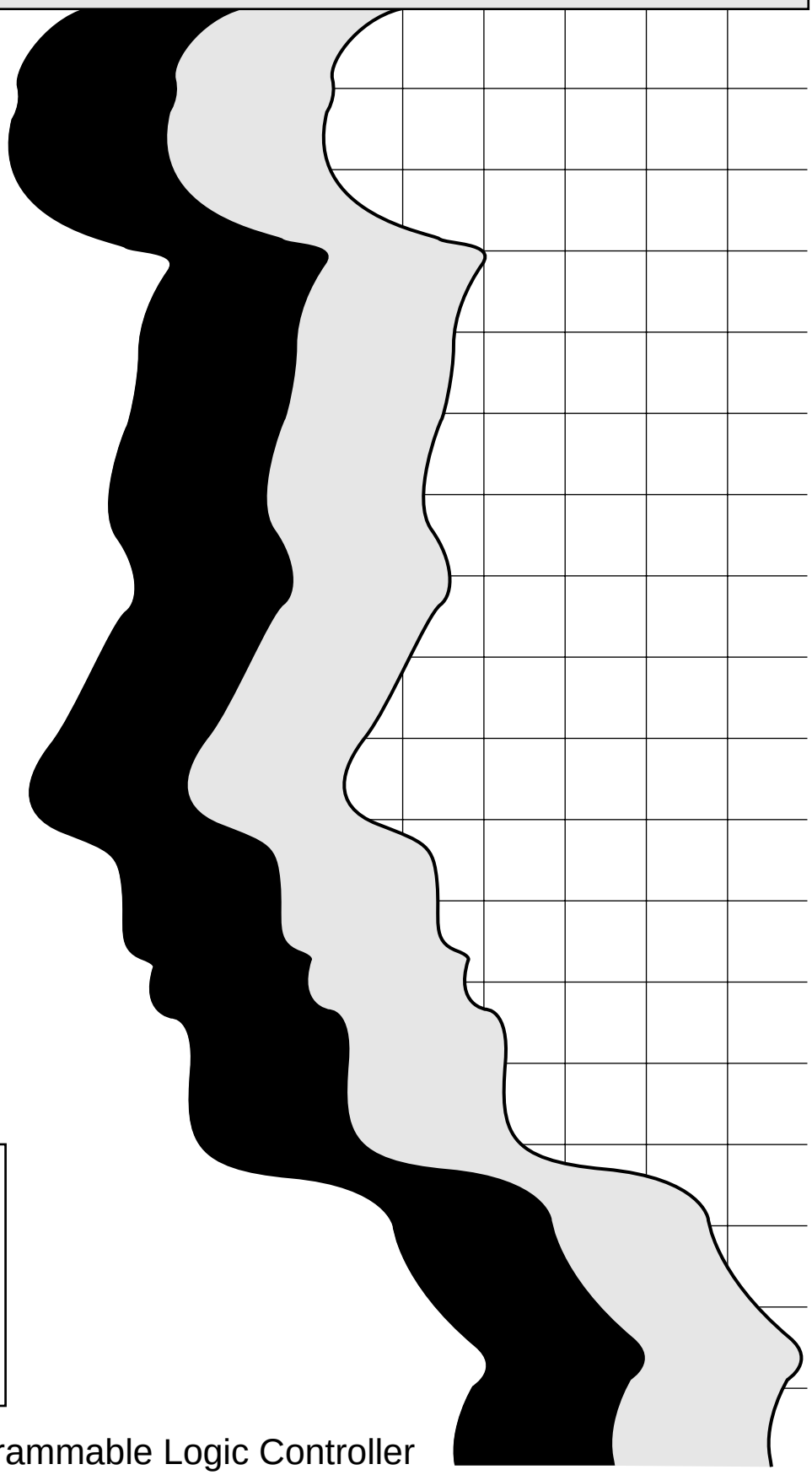
MITSUBISHI

Digital-Analog Converter Module Type A64DAVC/A64DAIC

User's Manual



A

MELSEC

Mitsubishi Programmable Logic Controller

● SAFETY PRECAUTIONS ●

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual.
Also pay careful attention to safety and handle the module properly. These precautions apply only to Mitsubishi equipment. Refer to the CPU module user's manual for a description of the PLC system safety precaution.
These ● SAFETY PRECAUTIONS ● classify the safety precautions into two categories: "DANGER" and "CAUTION".

⚠ DANGER	**Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.**
⚠ CAUTION	**Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carried out properly.**

Depending on circumstances, procedures indicated by ⚠ **CAUTION** may also be linked to serious results.
In any case, it is important to follow the directions for usage.
Store this manual in a safe place so that you can take it out and read it whenever necessary. Always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Install a safety circuit external to the PLC that keeps the entire system safe even when there are problems with the external power supply or the PC module. Otherwise, trouble could result from erroneous output or erroneous operation.
  (1) Outside the PLC, construct mechanical damage preventing interlock circuits such as emergency stop, protective circuits, positioning upper and lower limits switches and interlocking forward /reverse operations.
  (2) When the PLC detects the following problems, it will stop calculation and turn off all output.
    - The power supply module has over current protection equipment and over voltage protection equipment.
    - The PLC CPUs self-diagnostic functions, such as the watchdog timer error, detect problems. In addition, all output will be turned on when there are problems that the PLC CPU cannot detect, such as in the I/O controller. Build a fail safe circuit exterior to the PLC that will make sure the equipment operates safely at such times. See user's manual for example fail safe circukts.

    See this user's manual for example fail safe circukts.
  (3) Output could be left on or off when there is trouble in the outputs module relay or transistor. So build an external monitoring circuit that will monitor any single outputs that could cause serious trouble.
- When overcurrent which exceeds the rating or caused by short-circuited load flows in the output module for a long time, it may cause smoke or fire. To prevent this, configure an external safety circuit, such as fuse.
- Build a circuit that tums on the external power supply when the PLC main module power is turned on. If the external power supply is turned on first, it could result in erroneous output or erroneous operation.
- When there are communication problems with the data link, the communication problem station will enter the following condition.
  Build an interlock circuit into the Sequence program that will make sure the system operates safely by using the communication state information. Not doing so could result in erroneous output or erroneoud operation.
  (1) For the data link data, the data prior to the communication error will be held.
  (2) The MELSECNET (II,/B,/10) remote I/O station will turn all output off.
  (3) The MELSECNET/MINI-S3 remote I/O station will hold the output or turn all output off depending on the E.C. remote setting.

  Refer to the data link manuals regarding the method for setting the communication problem station and the operation status when there are communication problem.
- When configuring a system, do not leave any slots vacant on the base. Should there be any vacant slots, always use a blank cover (A1SG60) or dummy module (A1SG62).
  When the extension base A1S52B, A1S55B or A1S58B is used, attach the dustproof cover supplied with the product to the module installed in slot 0.
  If the cover is not attached, the module's internal parts may be dispersed when a short-circuit test is performed or overdurrent/overvoltage is accidentally applied to the external I/O area.

⚠ CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other. They should be installed 100 mm (3.94 inch) or more from each other. Not doing so could result in noise that would cause erroneous operation.
- At the time of power ON or OFF, a voltage or current may be instantaneously output from output terminals. Therefore, ensure stable analog outputs before starting the control.

[DESIGN PRECAUTIONS]

⚠ CAUTION

- When controlling items like lamp load, heater or solenoid valve using an output module, large current (approximately ten times greater than that present in normal circumstances) may flow when the output is turned OFF→ON. Take measures such as replacing the module with one havingsufficient rated current.

[INSTALLATION PRECAUTIONS]

⚠ DANGER

- Use the PLC in an environment that meets the general specifications contained in this manual. Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.
- Install so that the pegw on the bottom of the module fit securely into the base unit peg holes, and use the specified torque to tighten the module's fixing screws. Not installing the module correctly could reault in erroneous operation, damage, or pieces of the product falling.
- Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.
- When installing more cables, be sure that the base unit and the module connectors are installed correctly. After installation, check them for looseness. Poor connections could result in erroneous input and erroneous output.
- Correctly connect the memory cassette installation connector to the memory cassette. After installation, be sure that the connection is not loose. A poor connection could result in erroneous operation.
- Do not directly touch the module's conductive parts or electronic components. Doing so could cause erroneous operation or damage of the module.

[WIRING PRECAUTIONS]

⚠ DANGER

- Completely turn off the external power supply when installing or placing wiring. Not completely tuming off all power could result in electric shock or damage to the product.
- When tuming on the power supply or operating the module after installation or wiring work, be sure that the module's terminal covers are correctly attached. Not attaching the terminal cover could result in electric shockl.

⚠ CAUTION

- Be sure to ground the FG terminals and LG terminals to the protective ground conductor. Not doing so could result in electric shock or erroneous operation.
- Use applicable solderless terminals and tighten them with the specifiedtorque. If any solderless spade terminal is used, it may be disconnected when the terminal screw comes loose, resulting in failure.
- When wiring in the PLC, be sure that it is done correctly by checking the product's rated voltage and the terminal layout. Connecting a power supply that is different from the rating or incorrectly wiring the product could result in fire or damage.

[WIRING PRECAUTIONS]

⚠CAUTION

- Do not connect multiple power supply modules in parallel. Doing so could cause overheating, fire or damage to the power supply module. If the terminal screws are too tight, it may couse falling, short circuit or erroneous operation due to damage of the screws or module.
- Tighten the terminal screws with the specified torque. If the terminal screws are loose, it could result in short circuits, fire, or erroneous operation.
- Tightening the terminal screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module. Such debris could cause fires, damage, or erroneous operation.
- External connections shall be crimped or pressure welded with the specified tools, or correctly soldered. For information regarding the crimping and pressure welding tools, see the I/O module's user's manual. Imperfect connections could result in short circuit, fires, or erroneous operation.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠DANGER

- Do not touch the terminals while power is no. Doing so could cause shock or erroneous operation.
- Correctly connect the battery. Also, do not charge, disassemble, heat, place in fire, short circuit, or solder the battery. Mishandling of battery can cause overheating or cracks which could result in injury and fires.
- Switch all phases of the external power supply off when cleaning the module or tightening the terminal screws. Not doing so could result in electric shock. If the screws are too tight, it may cause falling, short circuit or erroneous operation due to damage of the screws or modules.
- Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

⚠CAUTION

- The online operations conducted for the CPU module being operated, connecting the peripheral device (especially, when changing data or operation status), shall be conducted after the manual has been carefully read and a sufficient check of safety has been conducted. Operation mistakes could cause damage or trouble of the module.
- Do not disassemble or modify the modules. Doing so could cause trouble, erroneous operation, injury, or fire.
- Switch all phases of the external power supply off beforw mounting or removing the module. If you do not switch off the external power supply, it will cause failure or malfunction of the module.
- Always use the designated fuse for replacement.
  Using a larger capacity fuse or wire could cause a fire.

[DISPOSAL PRECAUTIONS]

⚠CAUTION

- When disposing of this product, treat it as industrial waste.

REVISIONS

※The manual number is given on the bottom right of the top cover.

Print Date	*Manual Number	Revision
May, 1990	IB (NA) 66248-A	First edition
Apr., 2001	IB (NA) 66248-B	Addition SAFETY PRECAUTIONS, WARRANTY Correction Chapter 1, Section 2.1, 2.2.1, 2.2.2, 2.3.1, 2.3.2, 3.2.1, 3.3, 3.4, 3.5.4, 3.5.5, 4.4, 4.6.3, 4.6.4, 5.4, 5.6.1, 5.6.2, 5.6.4, 6.1, 6.2, 6.3, 6.4, 6.8.1, 6.9.2, 6.10.2, 7.1, Appendix 3
Mar., 2006	IB (NA) 66248-C	Correction SAFETY PRECAUTIONS, REVISIONS

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

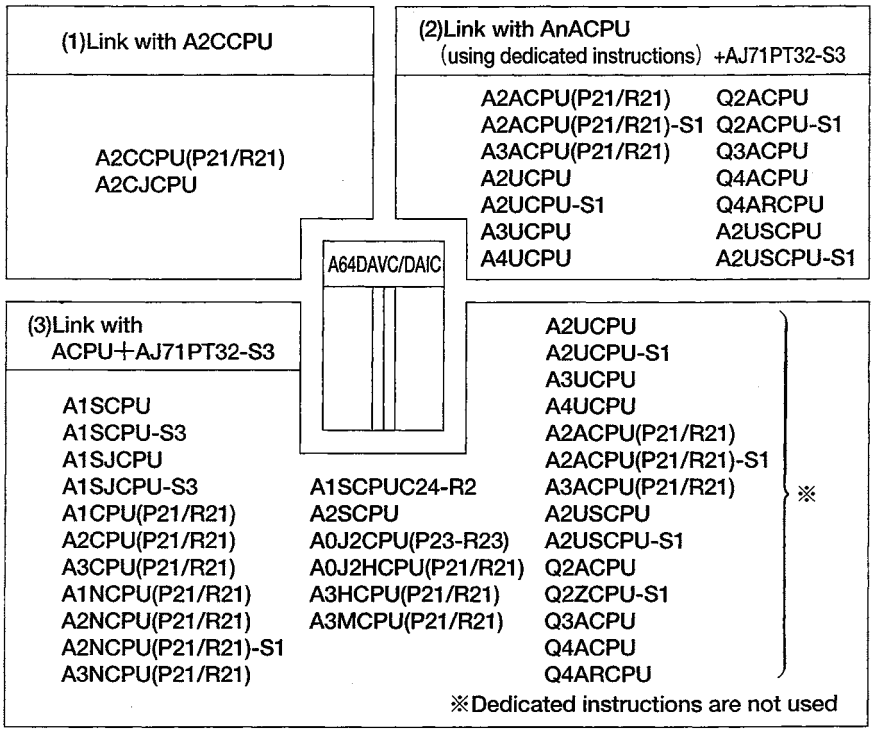
1. INTRODUCTION

This User's Manual describes the specifications, handling and programming procedures of the A64DAVC digital-analog converter module and the A64DAIC digital-analog converter module (hereinafter called "the A64DAVC/DAIC) to be used in combination with the A2CCPU or as remote stations in the MELSECNET/MINI-S3 data link system.

(1) A64DAVC
Used to convert incoming 16-bit signed binary data which are set with the PLC CPU to voltage outputs ranging from -10V to 10V for four channels.

(2) A64DAIC
Used to convert incoming 16-bit signed binary data which are set with the PLC CPU to current outputs ranging from 0mA to 20mA for four channels.

The following are the CPUs applicable to the paths for link with the A64DAVC/DAIC.



Please refer to the following manuals if necessary for the use of the A64DAVC/DAIC.

ACPU Programming Manual (Fundamentals) IB (NA) 66249
ACPU Programming Manual (Common Instructions) IB (NA) 66250
A2A(S1)/A3ACPU Programming Manual (Dedicated Instructions) IB (NA) 66251
A2CCPU User's Manual IB (NA) 66238
AJ71PT32-S3 MELSECNET/MINI-S3 Master Unit User's Manual IB (NA) 66217
SW0GP-MINIP Operating Manual IB (NA) 66226

1.1 Features

(1) Allows connection to external devices up to 4 channels.

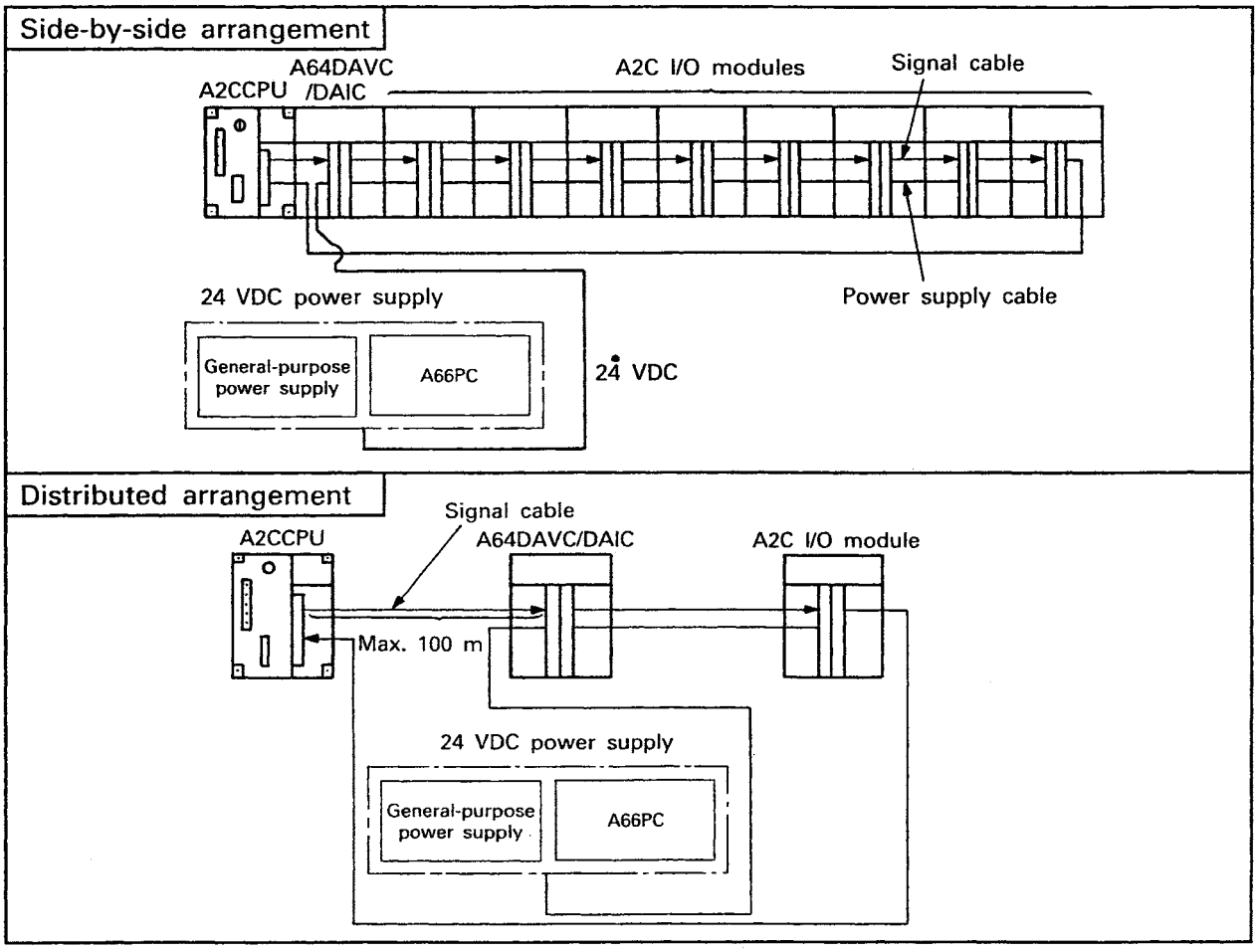
(2) Analog output enable/disable can be set independently for each channel.

(3) Analog output HOLD/CLEAR setting upon occurrence of CPU run stop or link errors is possible. (batch setting for all channels)

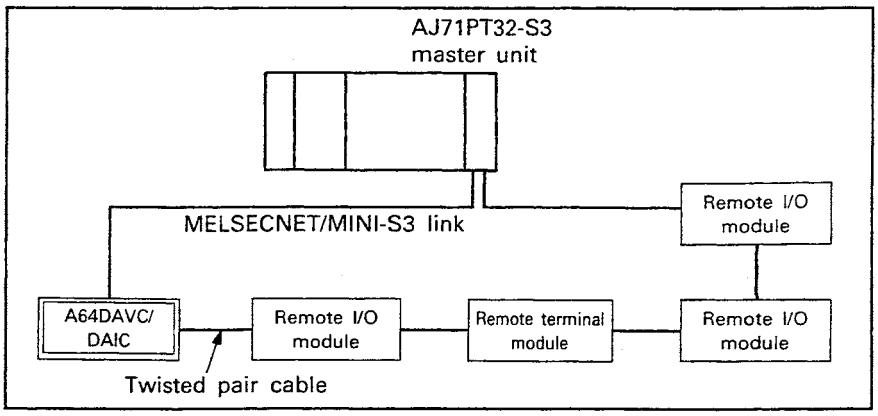
(4) Resolution of digital values can be set selecting from 1/4000, 1/8000 and 1/12000. (batch setting for all channels)

(5) Connects to the A2CCPU by flat cables, twisted pair cables or shielded PVC cables. Installation can be arranged as side-by-side or as distributed. The maximum length of cables connecting between the A68ADC and the A2CCPU in distributed arrangement is 100 m.

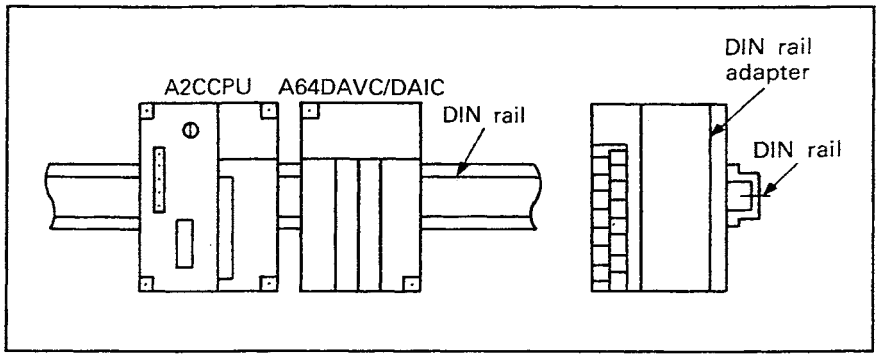
(6) Offset/gain setting can be set for each channel using the UP/DOWN switches.



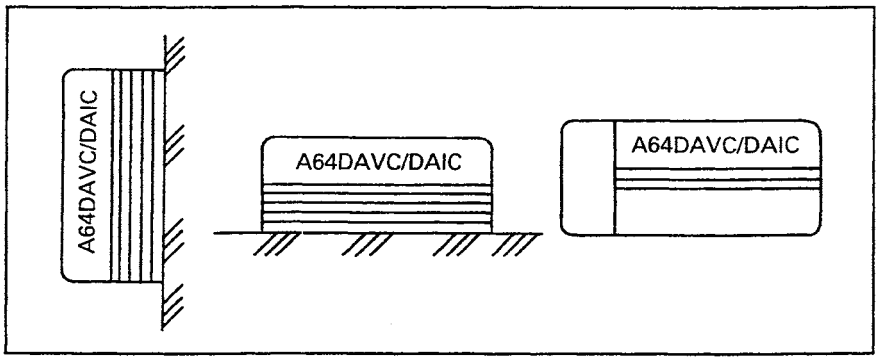
(7) Usable as a remote terminal module of the MELSECNET/MINI-S3 link.



(8) Can be mounted to the DIN rail using the DIN rail adapter.



(9) Designed compact: 170 mm high × 100 mm wide × 80 mm long. Can be mounted in a small space and in any position.



2. GENERAL SPECIFICATIONS

2.1 General Specifications

Table 2.1 shows the common specifications of various modules used.

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55℃</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">−20 to 75℃</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90% RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90% RH, non-condensing</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms to * JIS C 0911</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 55 Hz</td><td>——</td><td>0.075 mm (0.003 in)</td><td rowspan="2">10 times
*(1 octave/minute)</td></tr>
<tr><td>55 to 150 Hz</td><td>9.8m/s²</td><td>——</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to JIS C 0912 (98m/s² × 3 times in 3 directions)</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">500 VAC for 1 minute across DC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">5 MΩ or larger by 500 VDC insulation resistance tester across DC external terminals and ground</td></tr>
<tr><td>Operating ambience</td><td colspan="5">Free of corrosive gases. Dust should be minimal.</td></tr>
<tr><td>Cooling method</td><td colspan="5">Self-cooling</td></tr>
</table>

Table 2.1 General Specifications

REMARK

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10 Hz to 20 Hz, from 20 Hz to 40 Hz, from 40 Hz to 20 Hz, and 20 Hz to 10 Hz are referred to as one octave.

Note: * JIS: Japanese Industrial Standard

2.2 Specifications of A64DAVC

This section gives performance and function specifications of the A64DAVC.

2.2.1 Performance specifications

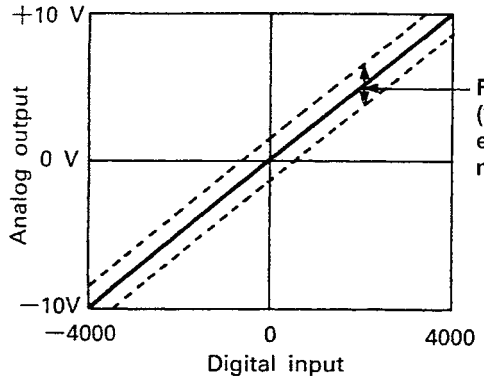
Table 2.2 shows the performance specifications of the A64DAVC.

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Digital output</td><td>(1) 16-bit signed binary data
(2) Setting range:
<table>
<tr><th>Resolution Setting</th><th>Setting Range</th></tr>
<tr><td>1/4000</td><td>−4000 to 4000</td></tr>
<tr><td>1/8000</td><td>−8000 to 8000</td></tr>
<tr><td>1/12000</td><td>−12000 to 12000</td></tr>
</table></td></tr>
<tr><td>Analog input</td><td>−10 to 0 to 10 VDC
(External load resistance: 2 KΩ to 1 MΩ)</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th rowspan="2"></th><th colspan="3">Digital Value Resolution</th><th rowspan="2">Analog Output*</th></tr>
<tr><th>1/4000</th><th>1/8000</th><th>1/12000</th></tr>
<tr><td rowspan="5">Digital input value</td><td>4000</td><td>8000</td><td>12000</td><td>+10 V</td></tr>
<tr><td>2000</td><td>4000</td><td>6000</td><td>+ 5 V</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0 V</td></tr>
<tr><td>−2000</td><td>−4000</td><td>−6000</td><td>− 5 V</td></tr>
<tr><td>−4000</td><td>−8000</td><td>−12000</td><td>−10 V</td></tr>
</table>
*When offset setting is 0 V and gain setting is 10 V.</td></tr>
<tr><td>*1 Maximum resolution of digital value</td><td>1/4000, 1/8000, 1/12000</td></tr>
<tr><td>*1 Overall accuracy
(Accuracy with respect to the maximum value)</td><td>±1.0% (±100mV)</td></tr>
<tr><td>*2 Maximum conversion speed</td><td>Maximum 25 ms/4 channels (same for 1 channel)
NOTE) Time from input of digital value till specified analog value (voltage) is output.</td></tr>
<tr><td>Analog output points</td><td>4 channels/module</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between out put terminals and PLC power
(no insulation between channels)</td></tr>
<tr><td>Occupied I/O stations (points)</td><td>4 stations (32 points)</td></tr>
<tr><td>Connection terminal</td><td>47-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm² (18 to 14 AWG) (Applicable tightening torque: 39~59N-cm</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>24 VDC internal current consumption</td><td>0.12</td></tr>
<tr><td>Weight kg (lb)</td><td>1.01</td></tr>
<tr><td>Outside dimensions mm(in)</td><td>170 (6.69) (H) × 100 (3.94) (W) × 80 (3.15) (D)</td></tr>
</table>

Table 2.2 Performance Specifications

*1 Overall accuracy

Overall accuracy is the accuracy when the output voltage setting is 10 volts.



*2 The maximum conversion speed is the conversion speed of the A64DAVC. The time from when the A64DAVC inputs the digital value from the PLC CPU until the end of the D/A conversion is the total of the PLC CPU time and the communication processing time.
For the communication processing time, refer to the processing times given CPU-by-CPU in Chapter 3 and later.

2.2.2 I/O conversion characteristics

(1) I/O conversion characteristics are indicated by an inclination connecting an offset value with a gain value set in test mode.

1) Offset/gain values

(a) Offset value

Voltage output from the A64DAVC when the digital value specified from the PLC CPU is "0".

(b) Gain value

Voltage output from the A64DAVC when the digital value specified form the PLC CPU is "4000" (when digital value resolusion setting is 1/4000).

(c) Offset/gain values are set before delivery as shown below.

Offset value: 0 V

Gain value: 10 V

Offset/gain values can be changed for each channel in the test mode. See Section 6.5 for offset/gain setting procedures.

2) The figure below shows an example of I/O conversion characteristics.

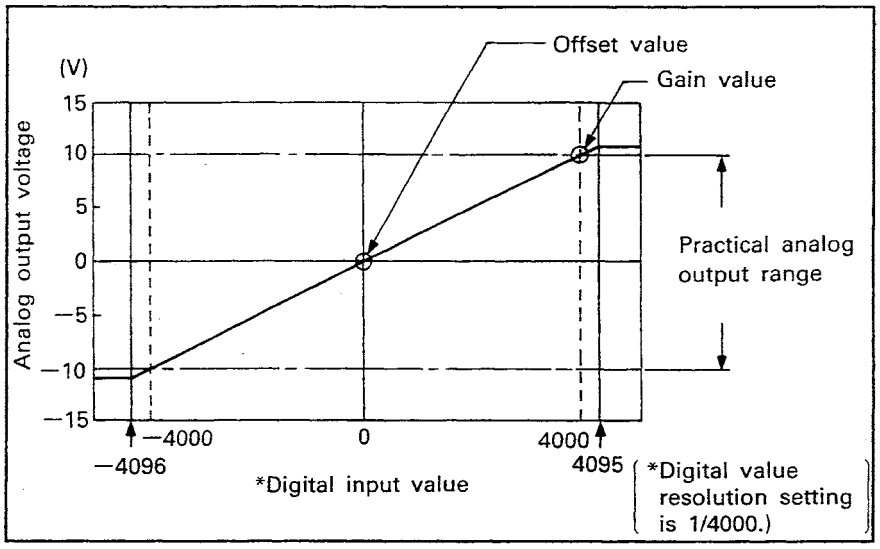


Fig. 2.1 I/O Conversion Characteristics

3) Relation between offset/gain values and analog output

Resolution of the A64DAVC can be changed as appropriate by offset/gain setting.

Resolution of analog value and analog output caused by digital input when offset/gain setting is changed are obtained as shown below.

$$\text{Resolution} = \frac{(\text{Gain value}) - (\text{Offset value})}{\text{Resolution of digital value}^{*1}}$$

$$\text{Analog output} = \frac{(\text{Gain value}) - (\text{Offset value})}{\text{Resolution of digital value}^{*1}} \times (\text{Digital input}) + (\text{Offset value})$$

$$= (\text{Resolution}^{*2}) \times (\text{Digital input}) + (\text{Offset value})$$

Value *1 varies with the set value of buffer memory address 8 (digital value resolution setting) of the A64DAVC. Use the values mentioned below.

Setting Data of Buffer Memory Address 8	Value *1 for Digital Value Resolution
1	4000
2	8000
3	12000

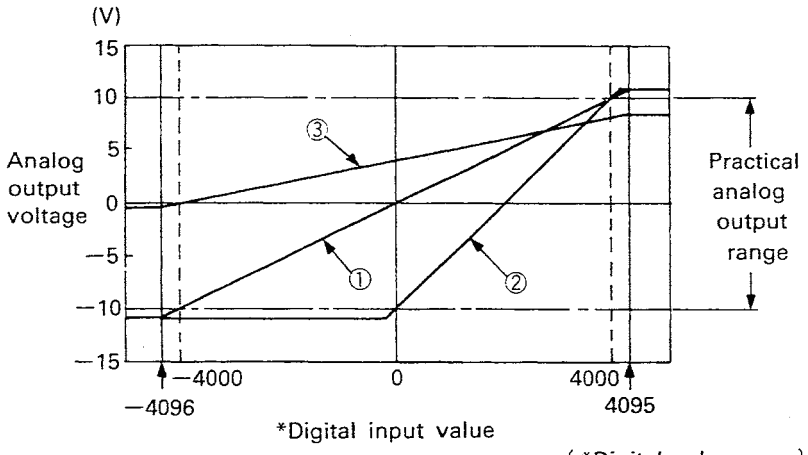
*2 The maximum resolution of the A64DAVC is provided as shown below. Variation in analog output when digital input is changed may sometimes be different from calculated value.

Output Voltage Range	Maximum Resolution
−10 to 0 to +10 V	0.7 mV

(2) The figures below show the I/O conversion characteristics when offset/gain setting is changed.

The relation between the following offset/gain settings and I/O conversion characteristics is shown on the right.

No.	Offset Value	Gain Value
①	0 V	+10 V
②	−10 V	+10 V
③	+4 V	+8 V



(*Digital value resolution setting is 1/4000.)

Example

The analog output voltages are as follows at the digital input value settings of 2000 and 500 for the characteristic graphs ① to ③.

No.	Digital Input Value	Analog Output Value
①	2000	+5.0 V
	500	+1.25 V
②	2000	0 V
	500	−7.5 V
③	2000	+6.0 V
	500	+4.5 V

Fig. 2.2 Offset/Gain Values vs. I/O Conversion Characteristics (10 V Setting)

2.3 Specifications of A64DAIC

This section gives performance and function specifications of the A64DAIC.

2.3.1 Performance specifications

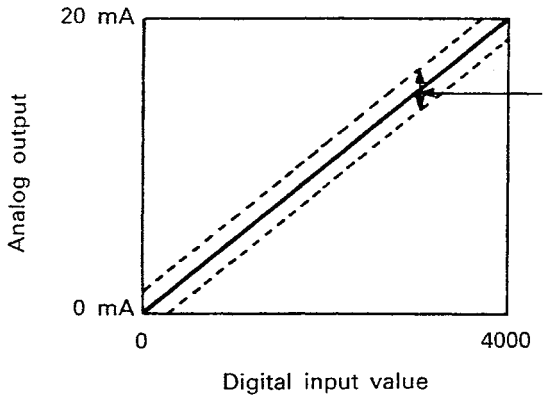
Table 2.3 shows the performance specifications of the A64DAIC.

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Digital output</td><td>(1) 16-bit signed binary data
(2) Setting range:
<table>
<tr><th>Resolution Setting</th><th>Setting Range</th></tr>
<tr><td>1/4000</td><td>0 to 4000</td></tr>
<tr><td>1/8000</td><td>0 to 8000</td></tr>
<tr><td>1/12000</td><td>0 to 12000</td></tr>
</table></td></tr>
<tr><td>Analog input</td><td>0DC to 20 mA
(External load resistance: 0 to 600 Ω)</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th rowspan="2"></th><th colspan="3">Digital Value Resolution</th><th rowspan="2">Analog Output*</th></tr>
<tr><th>1/4000</th><th>1/8000</th><th>1/12000</th></tr>
<tr><td rowspan="3">Digital input value</td><td>4000</td><td>8000</td><td>12000</td><td>+20 mA</td></tr>
<tr><td>2000</td><td>4000</td><td>6000</td><td>+12 mA</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>+ 4 mA</td></tr>
</table>
*When offset setting is 4 mA and gain setting is 20 mA.</td></tr>
<tr><td>*1 Maximum resolution of digital value</td><td>1/4000, 1/8000, 1/12000</td></tr>
<tr><td>*1 Overall accuracy
(accuracy with respect to the maximum value)</td><td>±1.0% (±200 μA)</td></tr>
<tr><td>*2 Maximum conversion speed</td><td>Maximum 25 msec/4 channels (same for 1 channel)
NOTE) Time from input of digital value till specified analog value (current) is output.</td></tr>
<tr><td>Analog output points</td><td>4 channels/module</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between output terminals and PLC power
(no insulation between channels)</td></tr>
<tr><td>Occupied I/O stations (points)</td><td>4 stations (32 points)</td></tr>
<tr><td>Connection terminal</td><td>47-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG) (Applicable tightening torque: 39 to 59 N·cm</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>24 VDC internal current consumption</td><td>0.15</td></tr>
<tr><td>Weight kg (!b)</td><td>1.01</td></tr>
<tr><td>Outside dimensions mm(in)</td><td>170 (6.69) (H) × 100 (3.94) (W) × 80 (3.15) (D)</td></tr>
</table>

Table 2.3 Performance Specifications

*1 Overall accuracy

Overall accuracy is the accuracy when the output voltage setting is 20 mA.



*2 The maximum conversion speed is the conversion speed of the A64DAVC. The time from when the A64DAVC inputs the digital value from the PLC CPU until the end of the D/A conversion is the total of the PLC CPU time and the communication processing time.
For the communication processing time, refer to the processing times given CPU-by-CPU in Chapter 3 and later.

2.3.2 I/O conversion characteristics

(1) I/O conversion characteristics are indicated by an inclination connecting an offset value with a gain value set in test mode.

1) Offset/gain values
   (a) Offset value
   Voltage output from the A64DAIC when the digital value specified from the PLC CPU is "0".
   (b) Gain value
   Voltage output from the A64DAIC when the digital value specified form the PLC CPU is "4000" (when digital value resolusion setting is 1/4000).
   (c) Offset/gain values are set before delivery as shown below.
   Offset value: 4 mA
   Gain value: 20 mA
   Offset/gain values can be changed for each channel in the test mode. See Section 6.5 for offset/gain setting procedures.

2) The figure below shows an example of I/O conversion characteristics.

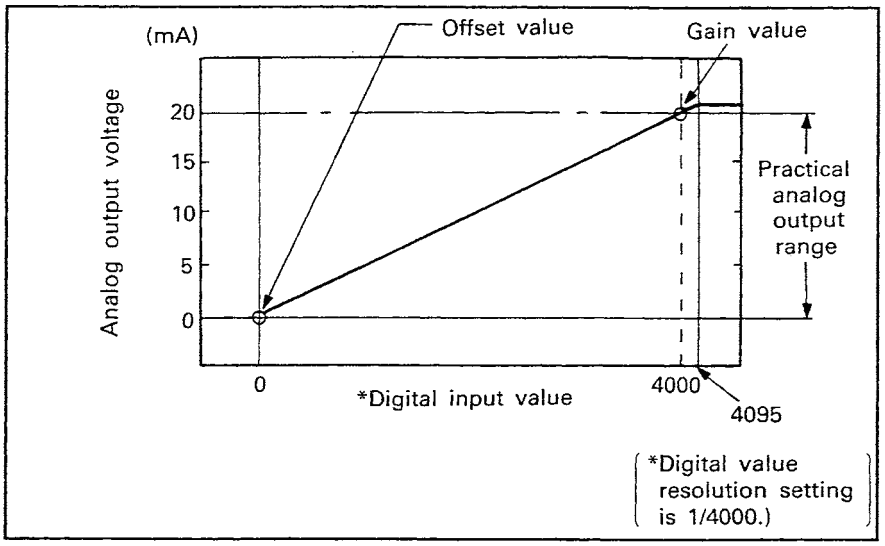


Fig. 2.3 I/O Conversion Characteristics

3) Relation between offset/gain values and analog output
Resolution of the A64DAIC can be changed as appropriate by offset/gain setting.
Resolution of analog value and analog output caused by digital input when offset/gain setting is changed are obtained as shown below.

$$\text{Resolution} = \frac{(\text{Gain value}) - (\text{Offset value})}{\text{Resolution of digital value}^{*1}}$$

$$\text{Analog output} = \frac{(\text{Gain value}) - (\text{Offset value})}{\text{Resolution of digital value}^{*1}} \times (\text{Digital input}) + (\text{Offset value})$$

$$= (\text{Resolution}^{*2}) \times (\text{Digital input}) + (\text{Offset value})$$

Value *1 varies with the set value of buffer memory address 8 (digital value resolution setting) of the A64DAIC. Use the values mentioned below.

Setting Data of Buffer Memory Address 8	Value *1 for Digital Value Resolution
1	4000
2	8000
3	12000

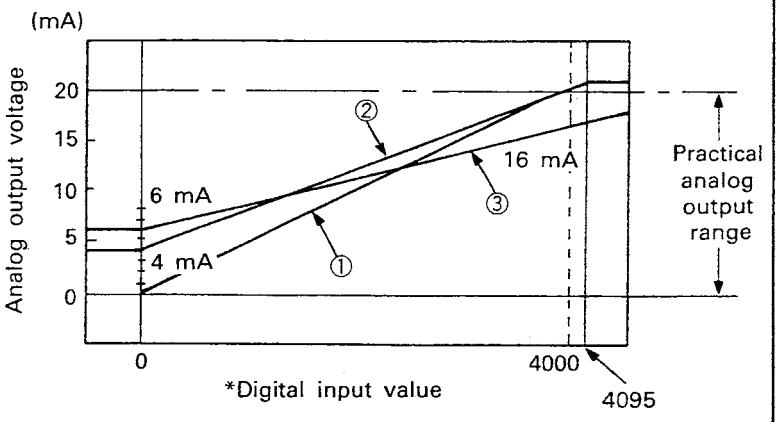
*2 The maximum resolution of the A64DAIC is provided as shown below. Variation in analog output when digital input is changed may sometimes be different from calculated value.

Output Current Range	Maximum Resolution
0 to 20 mA	2.86 μA

(2) The figures below show the I/O conversion characteristics when offset/gain setting is changed.

The relation between the following offset/gain settings and I/O conversion characteristics is shown on the right.

No.	Offset Value	Gain Value
①	0 mA	20 mA
②	4 mA	20 mA
③	6 mA	16 mA



(*Digital value resolution setting is 1/4000.)

Example

The analog output voltages are as follows at the digital input value settings of 2000 and 1000 for the characteristic graphs ① to ③.

No.	Digital Input Value	Analog Output Value
①	2000	10 mA
	1000	5 mA
②	2000	12 mA
	1000	8 mA
③	2000	11 mA
	1000	8.5 mA

Fig. 2.4 Offset/Gain Values vs. I/O Conversion Characteristics (10 V Setting)

2.4 Analog Output Control Functions

(1) Analog output HOLD/CLEAR setting (batch setting on 4 channels)
HOLD/CLEAR of analog output when the PLC CPU is stopped or the analog output enable signal is turned OFF is set with the HOLD/CLEAR terminals on the terminal block.
See Section 6.6 for setting procedures.

(2) Analog output enable signal (set by channel)
Output of whether analog value after D/A conversion or offset value is set for each channel with this signal (Y_{n+18} to Y_{n+1B})

(3) Analog output disable channel specification (set by channel)
Channels on which analog output is disabled can be set with buffer memory of the A64DAVC/DAIC. (When the A64DAVC/DAIC module is reset or powered on, analog output is enabled on 4 channels.)
For details, refer to "Assignment of buffer memory" in Sections 3 and after given in each type of CPU module.

(4) Analog output by respective combination of setting is as shown below.

Analog Output HOLD/CLEAR	CLEAR				HOLD	
Analog Output Enable Signal	Enable (ON)		Disable (OFF)		Enable (ON)/Disable (OFF)	
Analog Output Disable Channel Designation	Enable (0)	Disable (1)	Enable (0)	Disable (1)	Enable (0)	Disable (1)
Analog output at CPU RUN	Analog value after D/A conversion of digital value set with the PLC CPU is output.	0 V/0 mA	Offset value is output.	0 V/0 mA	Analog value after D/A conversion of digital value set with the PLC CPU is output.	0 V/0 mA
Analog output at CPU STOP	Offset value is output.	0 V/0 mA	Offset value is output.	0 V/0 mA	Analog value before STOP is held.	0 V/0 mA
Analog output at error occurrence	0 V/0 mA		0 V/0 mA		Analog value before error occurrence is held.	

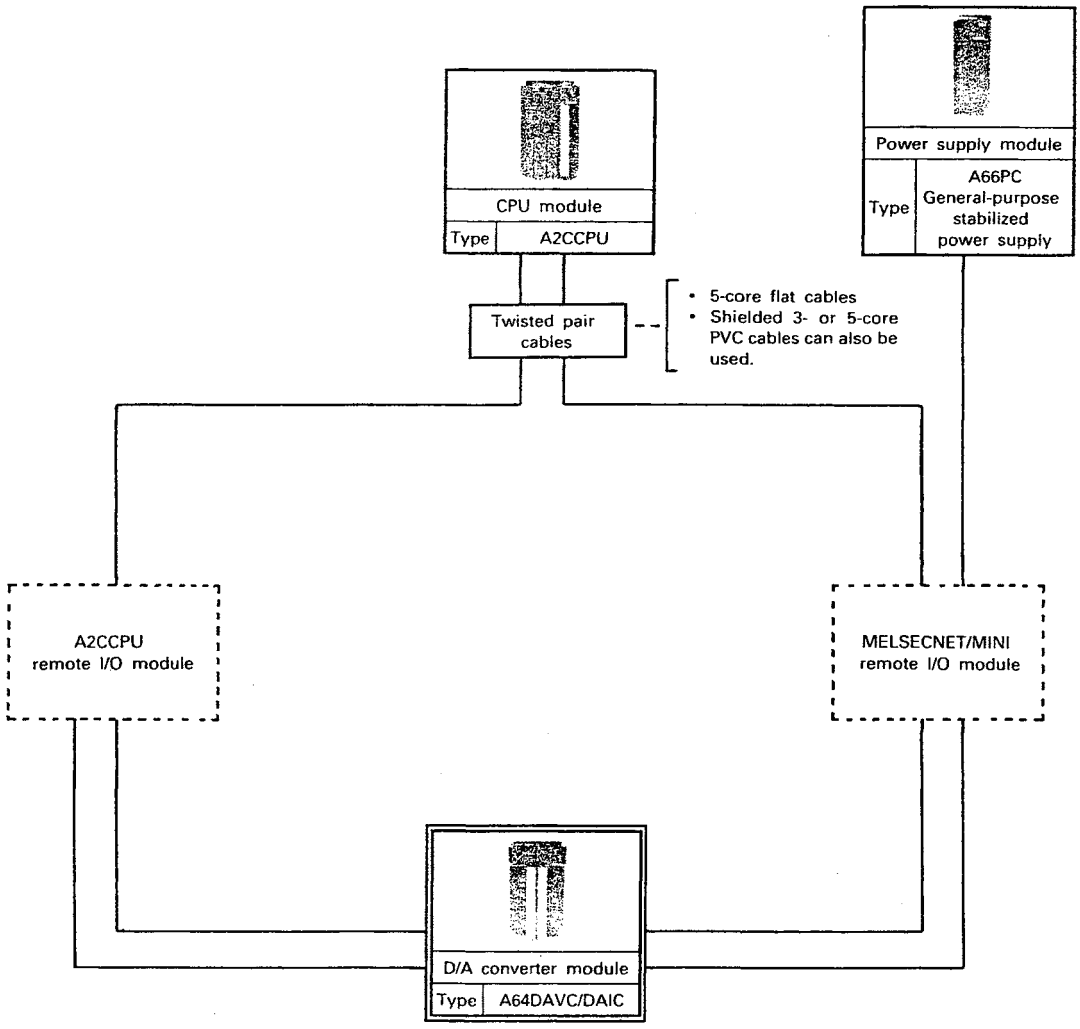
3. LINKING TO THE A2CCPU

The following sections describe the procedures to link the A68ADC to the A2CCPU. Booting systems SW4GP-GPPA, SW1S-GPPA or of previous type are equally applicable.

3.1 System Configuration

The following diagram shows when the A64DAVC/DAIC is used as a remote module of the A2CCPU.

3.1.1 Overall configuration



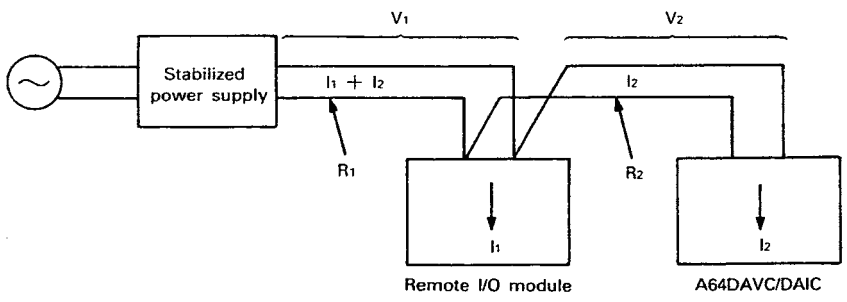
3.1.2 Cautions on constructing the system

(1) Flat cables, twisted pair cables and shielded 3- or 5-core PVC cables are used for connection between the A2CCPU and the A64DAVC/DAIC.
The maximum connecting distance between stations varies with cable size when twisted pair cables are used.

0.2 mm^2 to 0.5 mm^2 ····· 50 m
0.5 mm^2 and larger ····· 100 m

(2) The A64DAVC/DAIC requires external supply of 24 VDC power for internal power supply. Use the A66PC power supply module or a general-purpose stabilized power supply (24 VDC).

(3) When supplying power from one power supply to multiple A64DAVC/DAICs or to the remote I/O modules, select proper cables and wiring route taking voltage drop into consideration.



V_1: Voltage drop between stabilized power supply and remote I/O module
V_2: Voltage drop between remote I/O module and A64DAVC/DAIC
R_1: Resistance between stabilized power supply and remote I/O module
R_2: Resistance between remote I/O module and A64DAVC/DAIC
I_1: Remote I/O module current consumption
I_2: A64DAVC/DAIC current consumption

Calculation of voltage drop

$V_1 = R_1 \times (I_1 + I_2)$
$V_2 = R_2 \times I_2$

Receiving port voltage of remote I/O module

(Receiving port voltage of remote I/O module)
= (Voltage of stabilized power supply) − V_1

(A64DAVC/DAIC receiving port voltage)
= (Voltage of stabilized power supply) − V_1 − V_2

Connection is possible if the receiving port voltage of A64DAVC/DAIC is within the range 15.6 V through 31.2 V.

3.2 Data Communication Processings

3.2.1 Communication method

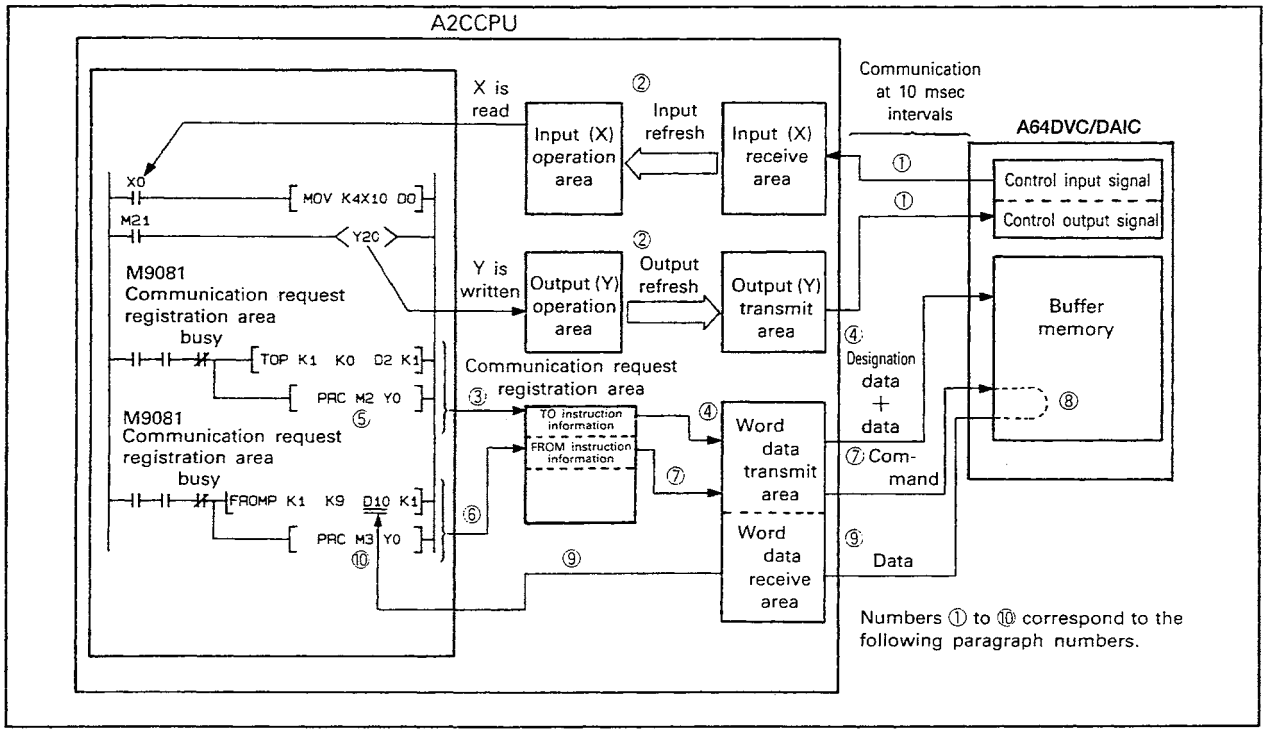


Fig. 3.1 Communication Processes

(1) Communication processes of control input/output signals used for interlocking of the A64DAVC/DAIC and the A2CCPU are described below. (See Section 3.3 for details of signals.)

① During sequence program execution, communication of input/output signals between the A2CCPU and the A64DAVC/DAIC is executed by suspending sequence program execution every 10 msec. During the communication, input signal data is stored in the input (X) receive area, and data stored in the output (Y) transmit area is output to the A64DAVC/DAIC.

② After the END instruction execution of the sequence program, data in the output (Y) operation area where operation result is stored is refreshed to the output (Y) transmit area, and then, data stored in the input (X) receive area is refreshed to the input (X) operation area.

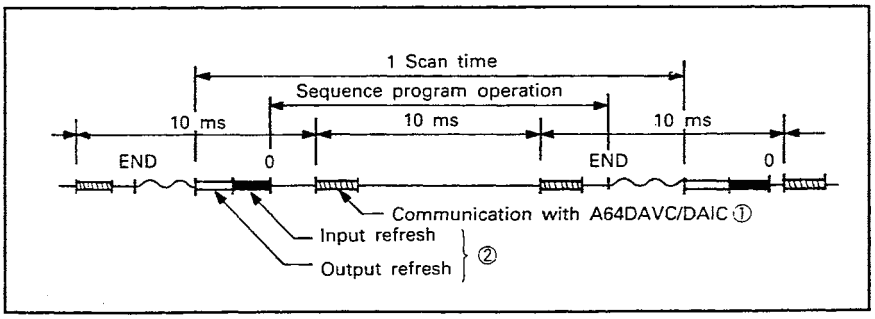


Fig. 3.2 Communication Timing of Input/output Signals

(2) Writing data to the A64DAVC/DAIC buffer memory

③ The TO instruction information is written to the communication request register area by the execution of the TO instruction, and registration of the TO instruction information is completed by execution of the PRC instruction. **When the transmission has started, the PLC CPU starts processing the following steps. (The PLC CPU does not wait for the response of transmission completion before starting processing the following steps.)**

④ By the execution of the PRC instruction, the TO instruction information stored in the communication request register area is transmitted in a few times of sending to the A64DAVC/DAIC via the word data transmit area after execution of the END instruction.

⑤ The communication completion flag (device M2 in Fig. 3.1) designated by the PRC instruction is turned ON for 1 scan from step 0 of the scan immediately after the response of communication completion sent from the A64DAVC/DAIC is received by the A2CCPU. Upon communication completion, the TO instruction information stored in the communication request register area is cleared.

(3) Reading data from the A64DAVC/DAIC buffer memory

⑥ The FROM instruction information is written to the communication request register area by the execution of the TO instruction, and registration of the FROM instruction information is completed by execution of the PRC instruction. **When the transmission has started, the PLC CPU starts processing the following steps. (The PLC CPU does not wait for the response of transmission completion before starting processing the following steps.)**

⑦ By the execution of the PRC instruction, the FROM instruction information stored in the communication request register area is transmitted in a few times of sending to the A64DAVC/DAIC via the word data transmit area after execution of the END instruction.

⑧ Upon receiving the FROM instruction information, the A64DAVC/DAIC sends data stored in the buffer memory of designated address back to the A2CCPU according to the information.

⑨ The read data is received by 1 word at 1 time of communication with the A64DAVC/DAIC and stored in the storage devices starting with that designated by the FROM instruction for the number of words designated.

⑩ The communication completion flag (device M3 in Fig. 3.1) designated by the PRC instruction is turned ON for 1 scan from step 0 of the scan immediately after the completion of storage of read data in designated devices.

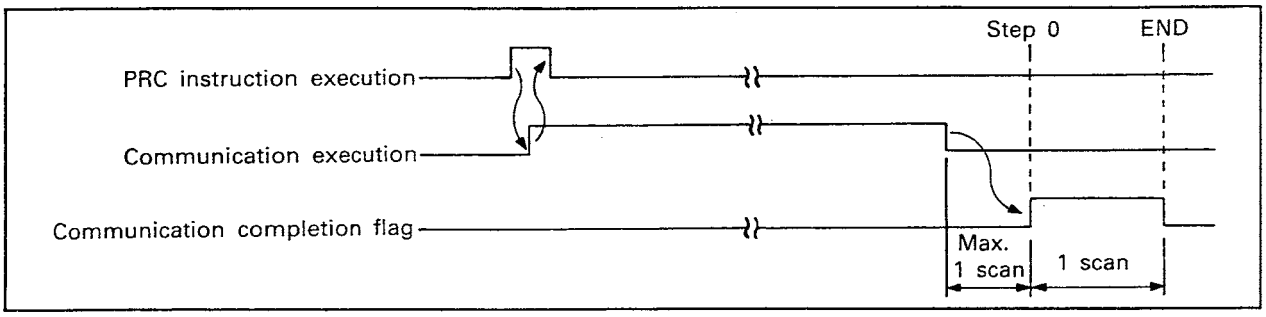


Fig. 3.3 Processing Timing of Data Reading and Writing

3.2.2 Processing time

(1) Data write time

Maximum processing time
= 2 scan time + 10 ms × (Number of write data words + 7) + *1 40 ms

(2) Data read time

Maximum processing time
= 2 scan time + 10 ms × (Number of read data words + 8) + *1 40 ms

*1: Internal processing time of the A64DAVC/DAIC

3.3 Input/output Signals Handled With the A2CCPU

Functions of the control input and output signals handled between the A64DAVC/DAIC and A2CCPU are described in this section. Devices X refer to the input signals from the A64DAVC/DAIC to the A2CCPU. Devices Y refer to the output signals from the A2CCPU to the A64DAVC/DAIC.
The actual device numbers for X/Y(n+0) to (n+1F) will differ from the setting number for the A68DAVC as shown on page 3-10.

Signal Direction: A64DAVC/DAIC → A2CCPU		Signal Direction: A2CCPU → A64DAVC/DAIC	
Device No.	Description	Device No.	Description
X(n+0) to X(n+3)	Unusable	Y(n+0) to Y(n+3)	Unusable
X(n+4)	The communication error detection flag which is set if a communication error occurs by execution of the FROM/TO instructions.	Y(n+4)	Communication error reset signal
X(n+5)	Reset switch ON detection flag of the A64DAVC/DAIC module	Y(n+5)	Reset switch ON detection flag reset signal
X(n+6)	Unusable	Y(n+6)	Unusable
X(n+7)	Communication completion response signal wait flag	Y(n+7)	Retransmission request signal
X(n+8) to X(n+17)	Unusable	Y(n+8) to Y(n+17)	Unusable
X(n+18)	D/A conversion READY (1) Turns ON when D/A conversion is ready in the normal mode (other than the test mode) after the A64DAVC/DAIC was turned on or the PLC CPU was reset. (2) Turns OFF when mode is switched from normal to test. (3) Used for the interlock for reading and writing from the PLC CPU to the A64DAVC/DAIC.	Y(n+18)	Analog output enable signal for channel 1 *1
		Y(n+19)	Analog output enable signal for channel 2 *1
		Y(n+1A)	Analog output enable signal for channel 3 *1
		Y(n+1B)	Analog output enable signal for channel 4 *1
X(n+19) to X(n+1F)	Unusable	Y(n+1C) to Y(n+1F)	Unusable

Table 3.1 List of Input/output Signals

POINT

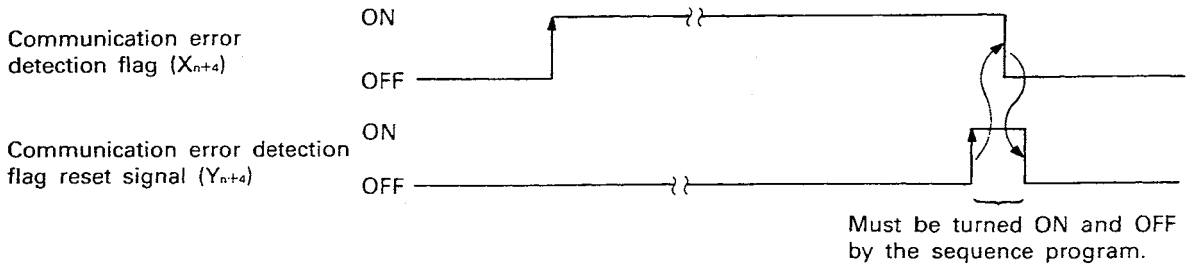
***1 Analog output enable signals ($Y_{(n+18)}$ to $Y_{(n+1B)}$) change in analog output condition between normal and test modes.**
(1) For analog output in normal mode, see Section 2.2.3 (3).
(2) In test mode, offset/gain values are output without regard to ON/OFF of the analog output enable signal of each channel.

IMPORTANT

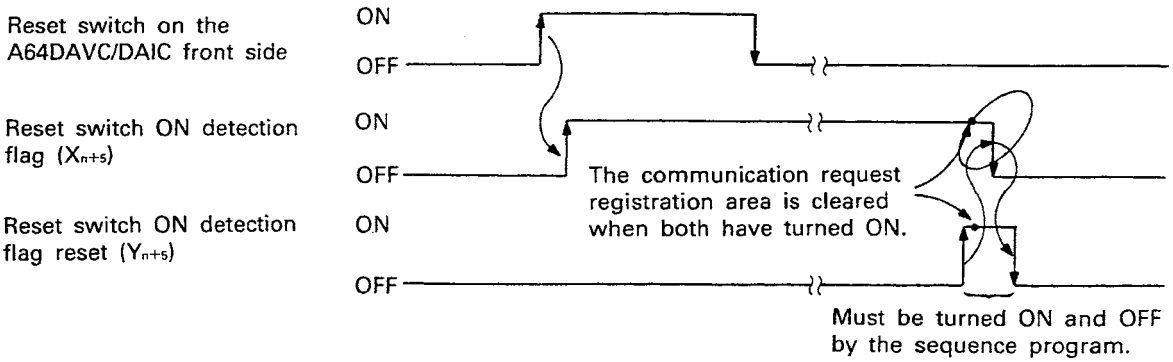
Devices $Y_{(n+0)}$ to $Y_{(n+3)}$, $Y_{(n+6)}$, $Y_{(n+8)}$ to $Y_{(n+17)}$ and $Y_{(n+1C)}$ to $Y_{(n+1F)}$ are unusable since they are used in the system.
If any of these devices are used (ON/OFF) in the sequence program, functions of the A64DAVC/DAIC are not guaranteed.

(1) Communication error detection flag (X_{n+4}) and communication error reset signal (Y_{n+4})
Turns ON (latched) when instruction data which cannot be read or written from the A2CCPU to the A64DAVC'DAIC is written. (The RUN LED of the A64DAVC/DAIC flickers.)
When X_{n+4} has turned ON, its error code (see Table 7.1 in Section 7.1) is stored in the error code storage area (special registers D9180 to D9193 of the A2CCPU) of corresponding remote terminal No.

To restart communication, turn ON the communication error reset signal (Y_{n+4}) with the sequence program and write "0" to address 9 of A64DAVC/DAIC to reset the A64DAVC/DAIC. Then the RUN LED illuminates.
When the communication error reset signal (Y_{n+4}) has turned ON, the error code in the error code storage area (D9180 to D9193) and corresponding FROM/TO instruction information stored in the communication request register area are cleared. (Also see (4) in this section.)



(2) Reset switch ON detection flag (X_{n+5}) and reset switch ON detection flag reset signal (Y_{n+5})
Turns ON (latched) when the reset switch of the A64DAVC/DAIC is moved to reset.
When both the reset switch ON detection flag and the reset switch ON detection flag reset signal have turned ON, the FROM/TO instruction information, stored in the communication request register area, with respect to corresponding remote terminal module is cleared.
However, if the retransmission request signal (Y_{n+7}) is ON, the communication request register area is not cleared.
To restart communication, turn ON the reset switch ON detection flag reset signal (Y_{n+5}) with the sequence program or reset the A2CCPU.

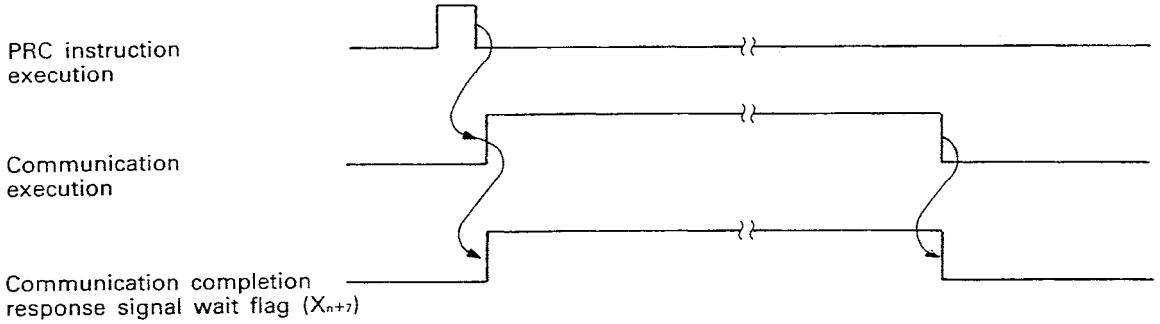


Point

(1) If the A64DAVC/DAIC is reset by moving the reset switch,it returns to the initial state. Start operation with initial setting.

(2) Since (X_{n+5}) turns ON also after the power is turned on, be sure to turn ON (Y_{n+5}) and OFF (X_{n+5}) at the initial stage. And then, execute programs for the A64DAVC/DAIC.

(3) Communication completion response signal wait flag (X_{n+7})
Turns ON when communication with the A64DAVC/DAIC is started by execution of the PRC instruction, and turns OFF when the communication completion response signal from the A64DAVC/DAIC is received.
Turns OFF also when the communication error reset signal (Y_{n+4}) has turned ON.



(4) Communication reset signal (Y_{n+7})
If the communication completion response signal with respect to the data transmitted by execution of the PRC instruction is not returned, the communication reset signal (Y_{n+7}) is turned ON to reset the A64DAVC/DAIC and the A2CCPU to the initial state.
(This resets communication state only to the initial state. Data set in the modules is not cleared.)

The input and output signals for controlling the A64DAVC/DAIC are in the range of X(Y)n + 0 to X(Y)n + 1F, occupying 4 stations (32 points).
Each station number is assigned in units of 8 points, and stations can be set from No. 1 to No. 64.
Table 3.3 shows input/output signal numbers and corresponding station numbers.

Station No.	Input/Output No.	Station No.	Input/Output No.	Station No.	Input/Output No.	Station No.	Input/Output No.
1	X/Y0~7	17	X/Y80~87	33	X/Y100~107	49	X/Y180~187
2	X/Y8~F	18	X/Y88~8F	34	X/Y108~10F	50	X/Y188~18F
3	X/Y10~17	19	X/Y90~97	35	X/Y110~117	51	X/Y190~197
4	X/Y18~1F	20	X/Y98~9F	36	X/Y118~11F	52	X/Y198~19F
5	X/Y20~27	21	X/YA0~A7	37	X/Y120~127	53	X/Y1A0~1A7
6	X/Y28~2F	22	X/YA8~AF	38	X/Y128~12F	54	X/Y1A8~1AF
7	X/Y30~37	23	X/YB0~B7	39	X/Y130~137	55	X/Y1B0~1B7
8	X/Y38~3F	24	X/YB8~BF	40	X/Y138~13F	56	X/Y1B8~1BF
9	X/Y40~47	25	X/YC0~C7	41	X/Y140~147	57	X/Y1C0~1C7
10	X/Y48~4F	26	X/YC8~CF	42	X/Y148~14F	58	X/Y1C8~1CF
11	X/Y50~57	27	X/YD0~D7	43	X/Y150~157	59	X/Y1D0~1D7
12	X/Y58~5F	28	X/YD8~DF	44	X/Y158~15F	60	X/Y1D8~1DF
13	X/Y60~67	29	X/YE0~E7	45	X/Y160~167	61	X/Y1E0~1E7
14	X/Y68~6F	30	X/YE8~EF	46	X/Y168~16F	62	X/Y1E8~1EF
15	X/Y70~77	31	X/YF0~F7	47	X/Y170~177	63	X/Y1F0~1F7
16	X/Y78~7F	32	X/YF8~FF	48	X/Y178~17F	64	X/Y1F8~1FF

Table 3.2 Input/output Signal Numbers and Corresponding Station Numbers

Example) The I/O numbers of controlling I/O signals when the A64DAVC/DAIC is set at station 5.

〈 I/O No. of A64DAVC/DAIC 〉		〈 I/O No. viewed from the PC CPU 〉
X/Y(n+0)		X/Y20
to	⇨	to
X/Y(n+1F)		X/Y3F

3.4 Assignment of Buffer Memory

Assignment of the A64DAVC/DAIC buffer memory (without battery backup) is shown below.

Address		Default	
0	CH1 Digital value setting area	0	Read/write from the PC CPU is possible.
1	CH2 Digital value setting area	0	
2	CH3 Digital value setting area	0	
3	CH4 Digital value setting area	0	
4	CH1 Analog output enable/disable setting area	0 (Enable)	
5	CH2 Analog output enable/disable setting area	0 (Enable)	
6	CH3 Analog output enable/disable setting area	0 (Enable)	
7	CH4 Analog output enable/disable setting area	0 (Enable)	
8	Digital resolution setting area	1 (1/4000)	
9	Error code storage area	0	

*All 16-bit data.

POINT

When the A64DAVC/DAIC has detected an error, the error code is stored in address 9, and the RUN LED flickers.

3.4.1 Contents and data configuration of the buffer memory

Contents of memory items and data configuration of the buffer memory are as follows.

(1) Digital value setting areas for CH1 to CH4 (Addresses 0 to 3)
  (a) Digital values for D/A conversion are written to these areas from the A2CCPU.
  (b) Setting ranges are as shown below.

Module	Digital Value Resolution Setting	Setting Range	Digital Value for D/A Conversion when Values Outside the Specified Ranges are Set.	
A64DAVC	1/4000	−4096 to 4095	−4097 and below: −4096	4096 and above: 4095
	1/8000	−8192 to 8191	−8193 and below: −8192	8192 and above: 8191
	1/12000	−12288 to 12287	−12289 and below: −12288	12288 and above: 12287
A64DAIC	1/4000	0 to 4095	−1 and below: 0	4096 and above: 4095
	1/8000	0 to 8191	−1 and below: 0	8192 and above: 8191
	1/12000	0 to 12287	−1 and below: 0	12288 and above: 12287

  (c) In the cases below, digital values for all channels for D/A conversion turn to default values.
    1) When the D/A conversion READY (X18) is turned ON after the A64DAVC/DAIC was powered on.
    2) When the D/A conversion READY (X18) is turned ON after the A64DAVC/DAIC module was reset.

(2) Analog output enable/disable setting areas for CH1 to CH4 (Addresses 4 to 7)
  (a) Used to set analog output enable/disable after D/A conversion.
  (b) Analog output enable/disable setting is done by writing 1 or 0 to corresponding setting area.
    • 0: Enable
    • 1: Disable

POINT

If a value other than 1 and 0 is written, analog output is processed according to the set data before writing, and the error code is stored in the error code storage area (address 9).

  (c) In the cases below, all channels are set for analog output enable. (Default)
    1) When the A64DAVC/DAIC is powered on.
    2) When the A64DAVC/DAIC module was reset.

(3) Digital value resolution setting area (Address 8)
  (a) Used to set digital value resolution with respect to analog output voltage range.
  Resolution setting is common to all channels.
  (b) Setting values are 1/4000, 1/8000 and 1/12000.
  Values 1, 2 and 3 are used with 1/4000 resolution as the standard value.

Example) To set resolution at 1/8000. (Write "2" in address 8.)

1/8000 = 1/4000 (standard) × 2

1/8000 resolution indicates the absolute value range of analog output voltage (0 to ±10 V).

−10 to 0 V, 0 to 10 V (1/8000) (1/8000) ⇨ −10 to 0 to 10 V (1/16000)

POINT

If a value other than 1, 2 and 3 is written, digital value resolution is processed according to the set data before writing or to default, and the error code is stored in the error code storage area (address 9).

  (c) In the cases below, digital value resolution is set at "1" (1/4000). (Default)
    1) When the A64DAVC/DAIC is powered on.
    2) When the A64DAVC/DAIC module was reset.

(4) Error code storage area (Address 9)

(a) When data is read from the PLC CPU, the A64DAVC/DAIC performs data range check and read/write area access checks once respectively. Any value outside the range is stored as error codes in 16-bit binary.
For details of error codes, see Section 7.1.

(b) When several error codes have occurred, the first error code detected by the A64DAVC/DAIC is stored, and the rest are not stored.

(c) To reset an error code, write 0 from the PLC CPU. If an error code is reset, the write data error code is set to "0" and the RUN LED of the A64DAVC/DAIC changes from flickering to illuminating.

3.5 Programming

This section describes the programming procedures when the A64DAVC/DAIC is used as a remote terminal of the A2CCPU.

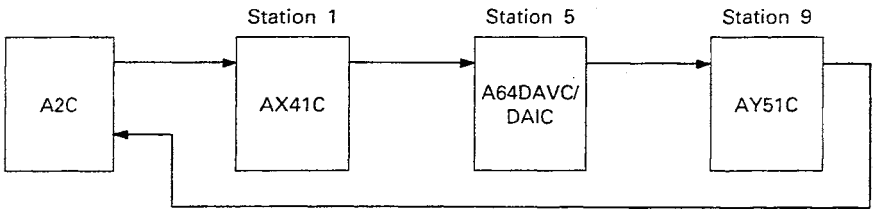
3.5.1 Initial setting of the A2CCPU

The A2CCPU allows connection of up to 14 remote terminals such as A64DAVC/DAIC modules. In order to use those remote terminals, it is necessary to set the remote terminal information in the A2CCPU in the initial setting.
This setting procedure varies with the system disk such as SW4GP-GPPA, SW1S-GPPA and the previous type used for booting. Table 3.3 shows the setting procedures including contents of setting and the differences between types of system disks.

Item	Setting range	Contents	Procedures	
			SW4GP-GPPA SW1S-GPPA	Previous type system FD
Total number of stations	1 to 64	Set the total number of stations including remote I/O modules and remote terminal modules.	Parameter setting	D9036
Head station number	1 to 61	Set the station number (head station number) set with the station number setting switch of each remote terminal module. (Example) A64DAVC/DAIC Set station number No. 1 AD61C Set station number No. 5 ⋮ No. 1 remote terminal module = 1 No. 2 remote terminal module = 5	Parameter setting	D9012 No. 1 remote terminal module D9022 No. 2 remote terminal module D9023 No. 3 remote terminal module ⋮ D9034 No. 14 remote terminal module
Protocol	0 to 1	Set the protocol used for data communication with remote terminal modules. 0: MINI standard protocol 1: No protocol Must be set at "0".	Parameter setting	D9035
Mode	0 to 2	Set the processings after line error return and at occurrence of line error. 0: Automatic online return enable 1: Automatic online return disable 2: Transmission stop at online error	Parameter setting	D9173

Table 3.3 Initial Setting Contents and Procedures

The following is an example program to write the initial setting data when the system is booted with a previous type system disk.

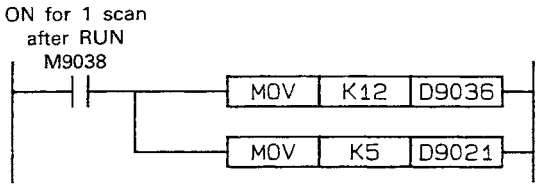


Total number of stations: AX41C: 4 stations
A64DAVC/DAIC: 4 stations
AY41C: 4 stations
4 + 4 + 4 = 12 stations

Head station number: Remote terminal module is A64DAVC/DAIC only.
No. 1 remote terminal: Station 5

Protocol: MINI standard protocol = 0 (default = 0)

Mode: Automatic online return enable = 0 (default = 0)



POINT

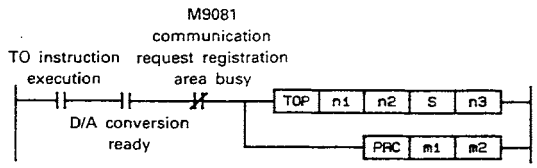
(1) If initial setting data has not been set, an SP. UNIT. ERR. (error No. 46) occurs and the CPU stops operation.

(2) If initial setting is done with both parameters and the sequence program while booting the system with the SW4GP-GPPA or SW1S-GPPA system disk, contents of parameter setting become valid and that set with the sequence program is ignored.

3.5.2 Writing data to the A64DAVC/DAIC

The TO instruction and the PRC instruction are handled as one block of instructions in the sequence program to write data to the buffer memory of designated remote terminal module.
Items to be written and procedures of writing to the A64DAVC/DAIC are described below.

(a) Digital value for each channel
(b) Analog output enable/disable setting for each channel
(c) Digital value resolution setting
(d) Write data error code clear



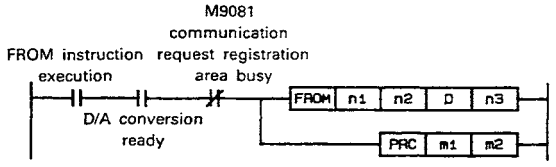
n_1	Head station number of remote terminal module
n_2	Head address of the buffer memory for writing
S	Head number of write data or of device which stores write data.
n_3	Number of write data
m_1	Device number to be turned ON for 1 scan when execution of the TO instruction is completed.
m_2	Dummy device number

For details of instructions, see the ACPU Programming Manual (Common Instructions).

3.5.3 Reading data from the A64DAVC/DAIC

The FROM instruction and the PRC instruction are handled as one block of instructions in the sequence program to read data from the buffer memory of designated remote terminal module.
Items to be read and procedures of reading from the A64DAVC/DAIC are described below.

(a) Write data error code

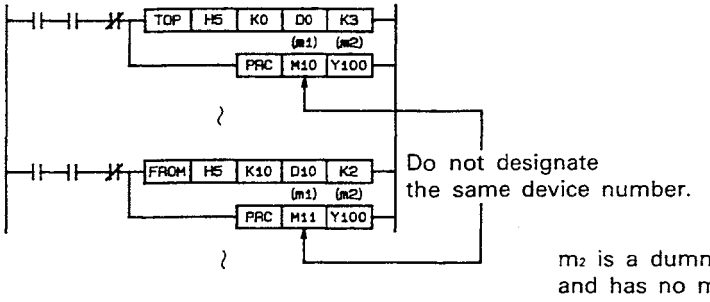


n_1	Head station number of remote terminal module
n_2	Head address of the buffer memory for reading
D	Head number of the device which stores read data.
n_3	Number of read data
m_1	Device number to be turned ON for 1 scan when execution of the FROM instruction is completed.
m_2	Dummy device No.

For details of instructions, see the ACPU Programming Manual (Common Instructions).

3.5.4 Cautions on programming

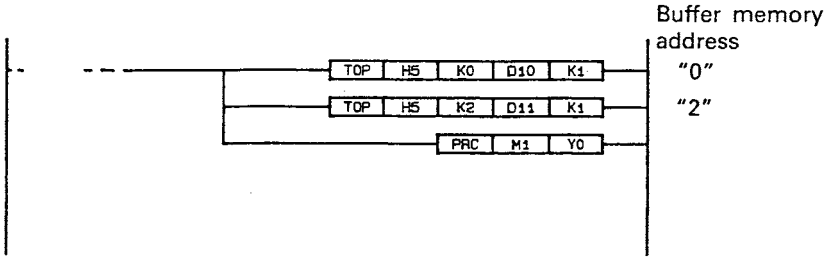
(1) It is necessary to provide the PRC instruction to the step immediately following the FROM/TO instruction. Use care not to designate same devices for "m_1" of the PRC instruction and for "m_1" of the PRC instruction provided to other step.



(2) The communication request registration areas can store up to 32 FROM/TO instructions. If the 33rd FROM/TO instruction is given, it is ignored without processing.
Provide an interlock with M9081 and D9081 so that the FROM/TO instruction may not be executed when the communication request registration areas are full.
M9081 and D9081 are described below.

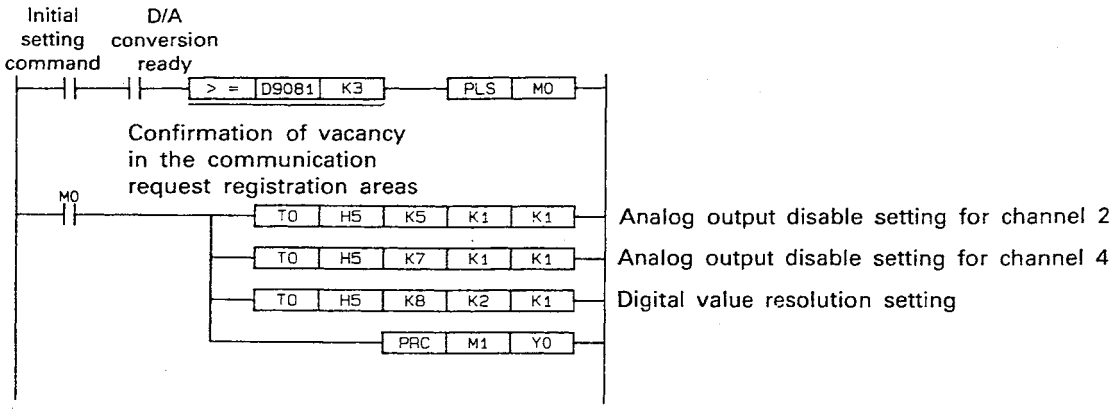
No.	Contents	Details
M9081	OFF: Communication request registration area has a vacancy. ON: Communication request registration areas are full.	There are 32 communication request registration areas for remote terminals. Turns ON when all areas become full.
D9081	The number of vacant areas of the communication request registration area for remote terminals.	The number of vacant areas of the communication request registration area is stored.

When data is written to two or more addresses in the buffer memory of the A64DAVC/DAIC, one FROM/TO instruction can execute data write if the addresses are continuous. If the addresses are not continuous, it is necessary to execute the FROM/TO instruction at two or more points (see below). In this case, the FROM/TO instruction information is stored in the communication request registration areas in plural.

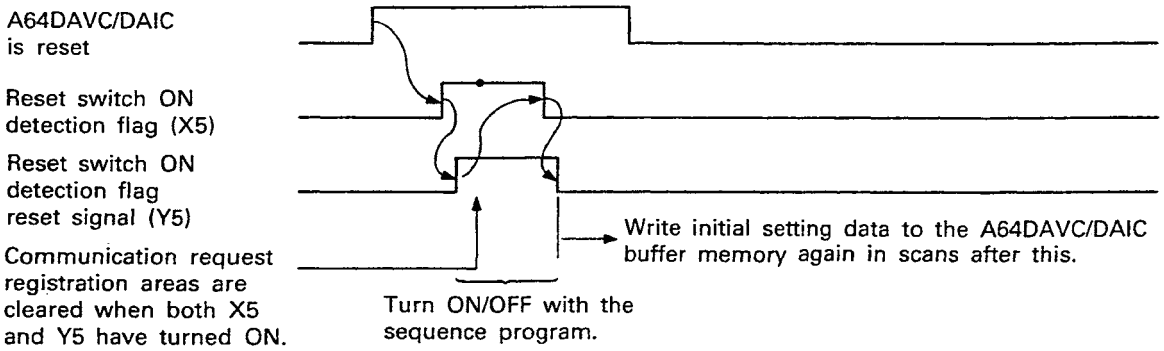


If an attempt is made to store the FROM/TO instruction information which is larger than the number of vacant areas of communication request registration areas, such attempt is ignored. To prevent this, it is necessary to provide a condition to allow confirmation that the vacancy in the communication request registration areas is larger than the number of FROM/TO instruction information. The programming example shown below describes the case when the FROM/TO instruction is executed after confirming the vacancy in the communication request register areas.

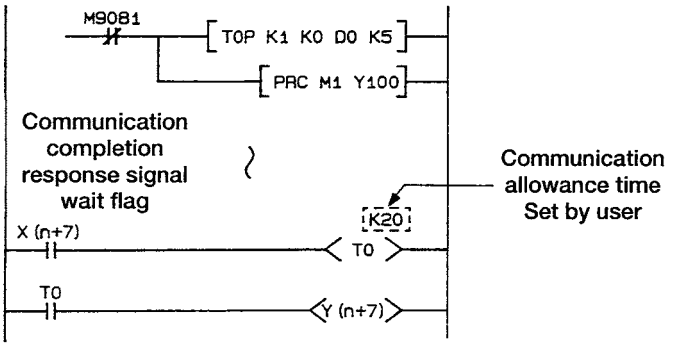
(Example) Initial setting program to the A64DAVC/DAIC
(Channels 2 and 4 are set for analog output disable. (Addresses 5 and 7)
Digital value resolution is set at 2 (1/8000).)



(3) When the reset switch on the front of the A64DAVC/DAIC is moved to reset, the A64DAVC/DAIC returns to initial state and performs D/A conversion with defaults.
Monitor the reset switch ON detection flag (X5) with a sequence program and, when the flag has turned ON, write initial setting data again to the A64DAVC/DAIC. (when D/A conversion is executed with other than defaults.)



(4) If a communication completion response signal to the transmission executed to the A64DAVC/DAIC is not sent back, the CPU module is set in the state waiting for the communication completion signal infinitely unless the CPU module is reset. To prevent such a problem, provide a monitoring timer to allow retransmission of the same data at preset time intervals.

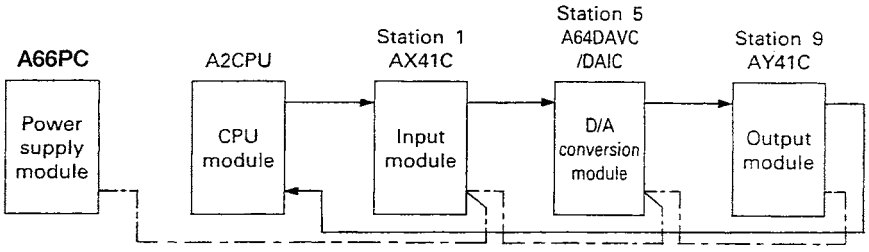


Provide the above circuit one block for each remote terminal module.

X(n+7) and Y(n+7) are control I/O signals for the A64DAVC/DAIC. See Section 3.3 for details.

3.5.5 Program example

The program example shown in this section writes the value (0 to 8000) set by the digital switch to channel 1 of the A64DAVC/DAIC in the following system configuration.
The resolution of the digital value is assumed to be 1/8000 and channels 2 to 4 to be disabled for analog output.

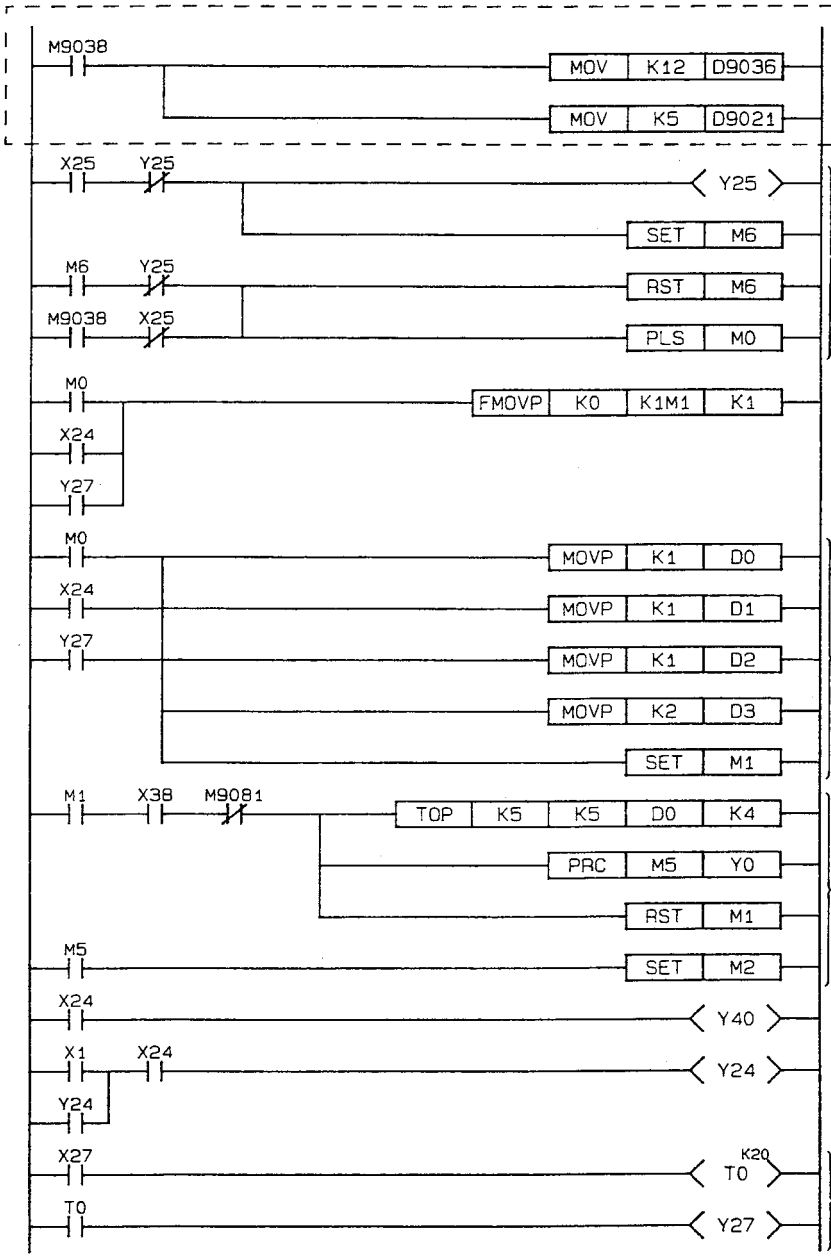


1) I/O numbers See Section 3.3.

A64DAVC/DAIC's I/O numbers		I/O numbers assigned by CPU
X/Y(n+0) to X/Y(n+1F)	⇨	X/Y20 to X/Y3F

2) A2CCPU's remote terminal settings (set to parameters) See Section 3.5.1.
   Total number of stations : 12
   Head station number : No. 1 remote terminal unit = station 5
   Protocol : MINI-standard protocol
   Mode : Online automatic return

3) Program example
   - Starting the CPU module run disables channels 2 to 4 for analog output and switching "on" X0 (digital value setting command) of the input module writes the values of X10 to X1F (digital value setting, BCD 4 digits) to the A64DAVC/DAIC.
   - Any digital value setting greater than 8000 switches "on" Y41 of the output module and is displayed by an external device.
   - Detection of a communication error with any remote terminal unit switches "on" Y40 to stop all processings.
   - Switching "on" X1 (error detection reset command) clears all the error status area and flags.
   - Resetting the A64DAVC/DAIC stops all processings. Switching "on" X25 (reset switch "on" detection flag) clears all.



If the When the conventional system disk is used, initial data is set by the circuit shown on the left.
(Set to parameters when SW4GP-GPPA or SW1S-GPPA is used.)

Switches on initial setting write command (M0) when A64DAVC/DAIC hardware reset is performed or CPU module run is started.

Resets M1-M4 if A64DAVC/DAIC hardware reset, communication error or communication response monitoring time-out occurs.

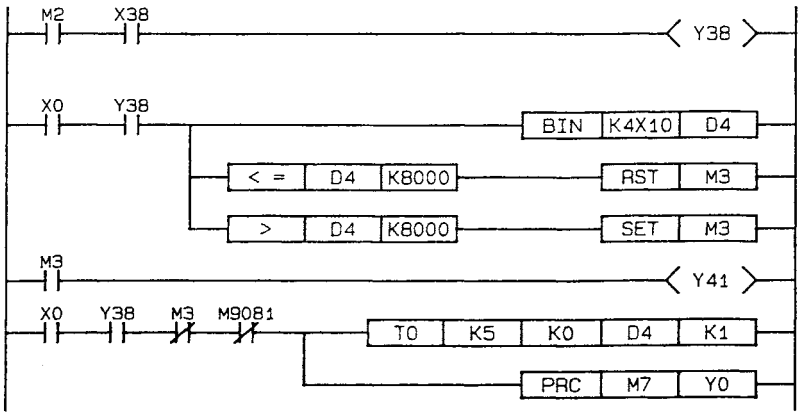
Stores A64DAVC/DAIC's initial setting data to D0 to D3 if initial setting write command, communication error reset or communication response monitoring time-out reset occurs.

D0 to D2: Disable CH2 to 4 for analog output.
D3: Sets digital value resolution to 1/8000.

Writes initial setting data stored in D0 to D3 to A64DAVC/DAIC buffer memory addresses 5 to 8 and sets M2.
Displays communication error on external device.

Stores error code into D9180.
Resets communication error when communication error reset command (X1) is switched on.

Resets communication error when communication response monitoring time-out occurs in communication response monitoring timer set by user.



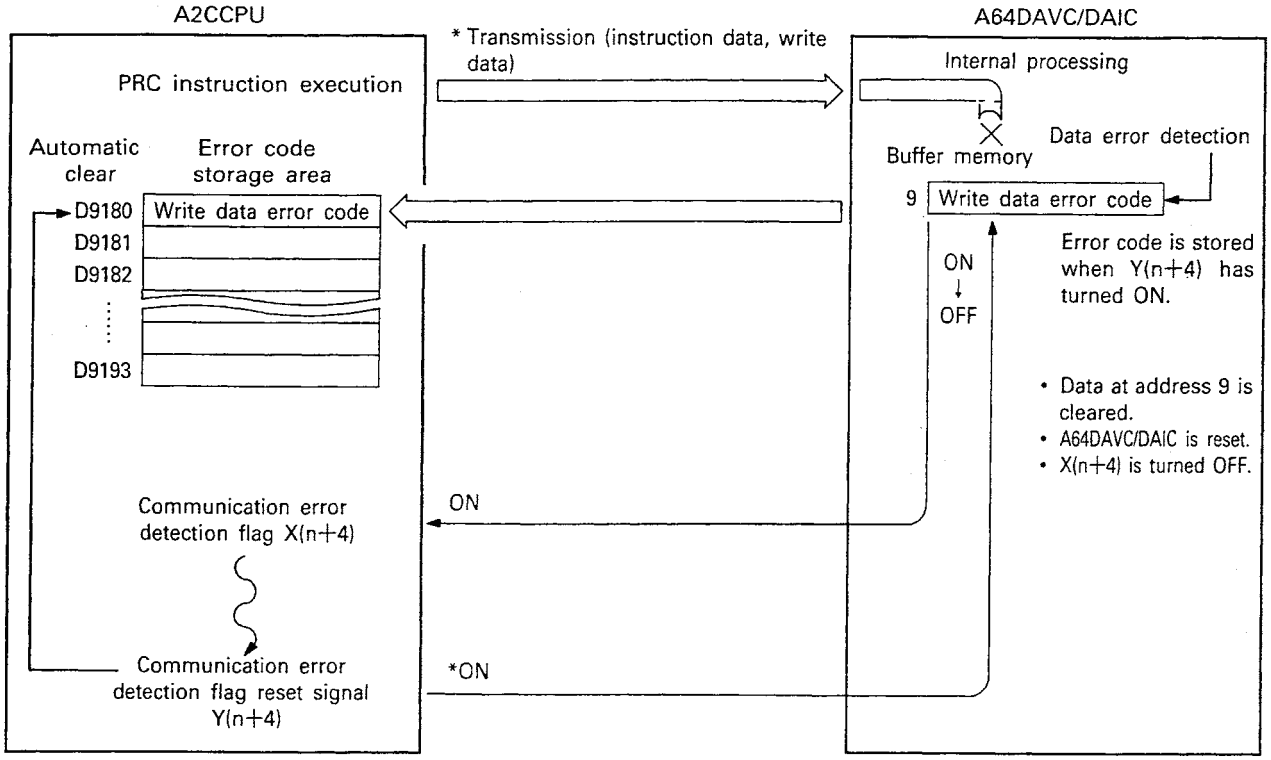
Switches on CH1's analog output enable signal when A64DAVC/DAIC's initial setting write is complete and D/A conversion is ready.

Converts inputs (X10 to X1F) from BCD digital switch into binary and stores results into D4 when digital value setting command (X0) is switched on.
Checks setting range of data stored in D4, and if data is outside setting range, switches on M3 and provides external display (Y41).

Writes D4 data to A64DAVC/DAIC buffer memory address 0 if D4 data is within setting range when digital value setting command (X0) is switched on.

3.6 Error Detection

The figure below shows how an error is detected when the A2CCPU and the A64DAVC/DAIC are used together.



*Processings marked by an asterisk are executed by the sequence program.

4. LINKING TO THE AnACPU AND THE AJ71PT32-S3

This section gives the linking procedures when dedicated instructions to the MELSECNET/MINI-S3 (master station is AJ71PT32-S3) of the AnACPU are used and the communication of control I/O signals with the A64DAVC/DAIC is set for automatic refresh. Use the SW4GP-GPPA or SW1S-GPPA system disk for booting.

IMPORTANT

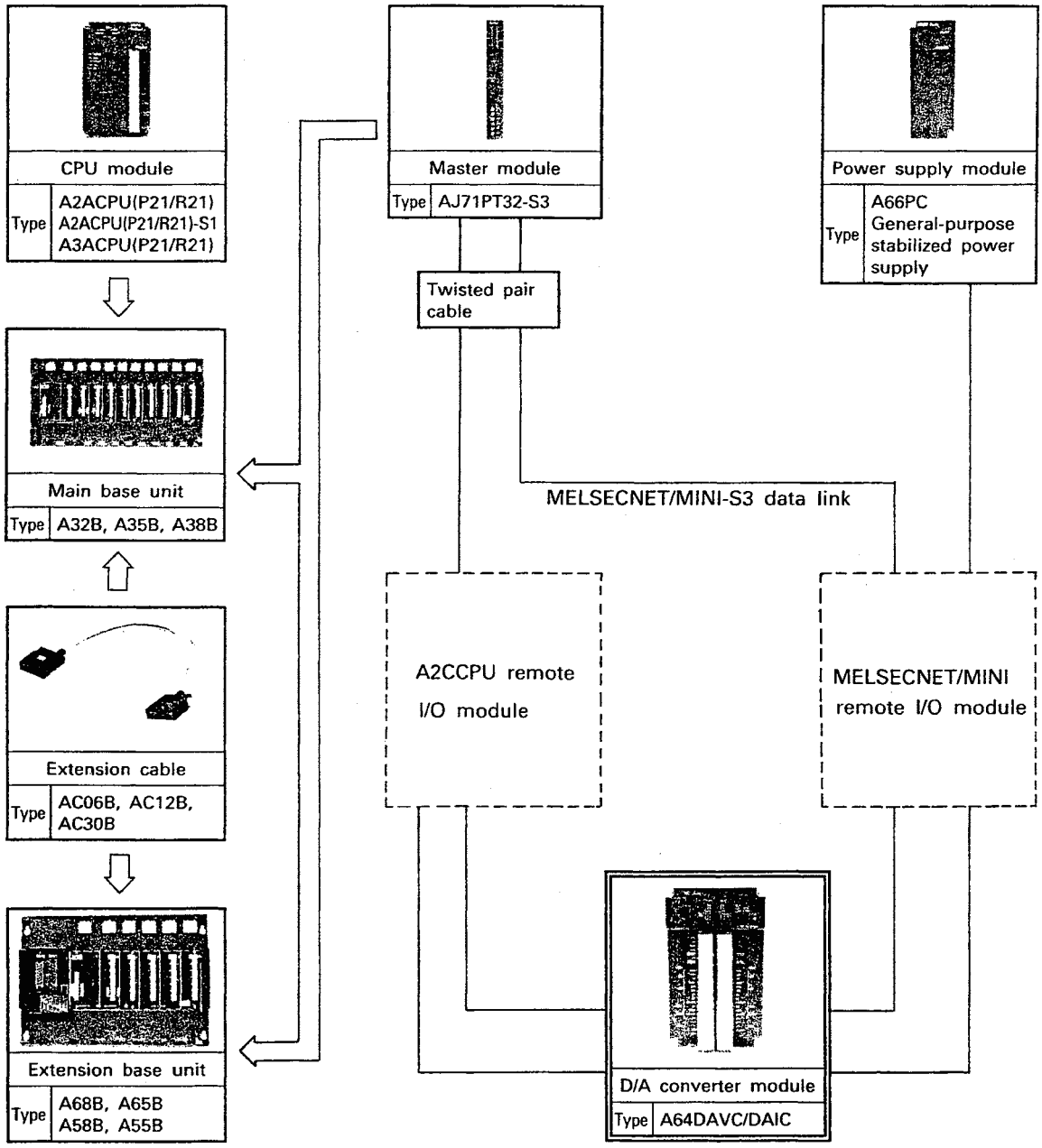
If dedicated instructions are used, the communication of control I/O signals with the A64DAVC/DAIC must be set for automatic refresh.

The linking procedures when dedicated instructions are not used are the same as those when a CPU other than the AnACPU is used. See Section 5 for details.

4.1 System Configuration

The following diagram shows when the A64DAVC/DAIC is used as a remote terminal module of the MELSECNET/MINI-S3 with the AJ71PT32-S3 master module linked to the A2ACPU, A2ACPU-S1 or A3ACPU.

4.1.1 Overall configuration



4.1.2 Applicable system modules

The A64DAVC/DAIC can be used as a remote terminal module of the MELSECNET/MINI-S3 link with the AJ71PT32-S3 as its master module.

(1) A maximum of 14 remote terminal modules such as the A64DAVC/DAIC can be connected to an AJ71PT32-S3 module. The following types of modules are used as remote terminal modules.
- A68ADC (analog/digital converter module)
- AD61C (high speed counter module)
- A64DAVC (digital/analog voltage converter module)
- A64DAIC (digital/analog current converter module)
- AJ35PTF-R2 (RS232C interface module)
- AJ35PT-OPB-MI (mounting type operation box)
- AJ35T-OPB-PI (portable type operation box)

(2) Remote modules connected to the AJ71PT32-S3 can occupy up to 64 stations.

(3) The AJ71PT32-S3 can be connected to an independent CPU system or to the master station or a local station of the MELSECNET data link system. It cannot be connected to a remote I/O station.
The number of modules connected to one CPU module is not limited.

REMARK

For details of the MELSECNET/MINI-S3 link system, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

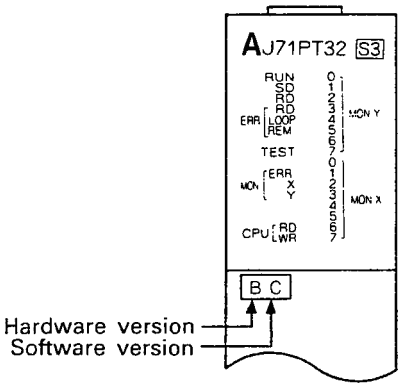
4.1.3 Cautions on constructing the system

(1) Twisted pair cables are used for connection between the AJ71PT32-S3 (master module) and the A64DAVC/DAIC.
The maximum connecting distance between stations varies with cable size when twisted pair cables are used.

0.2 mm^2 to smaller than 0.5 mm^2 ····· 50 m
0.5 mm^2 and larger ····· 100 m

(2) The A64DAVC/DAIC requires external supply of 24 VDC power for internal power supply. Use the A66PC power supply module or a general-purpose stabilized power supply (24 VDC). If one power supply is connected to two or more A68ADC or remote I/O modules, select proper cables and wiring route considering voltage drop due to cables.
Refer to Section 3.1.2 (3) for calculation of voltage drop.

(3) The AJ71PT32-S3 (master module) of which software version is C or later can be connected to the A64DAVC/DAIC. The modules of which software version is A, B or not specified on the front side cannot be used.



IMPORTANT

Use the AJ71PT32-S3 (master module) in the extension mode (48 occupied points). Be sure to mount the initial data ROM storing the total number of remote stations and remote terminal data (set station numbers of remote terminal modules and corresponding remote terminal numbers) to the master module.

4.2 Data Communication Processings

4.2.1 Communication processes

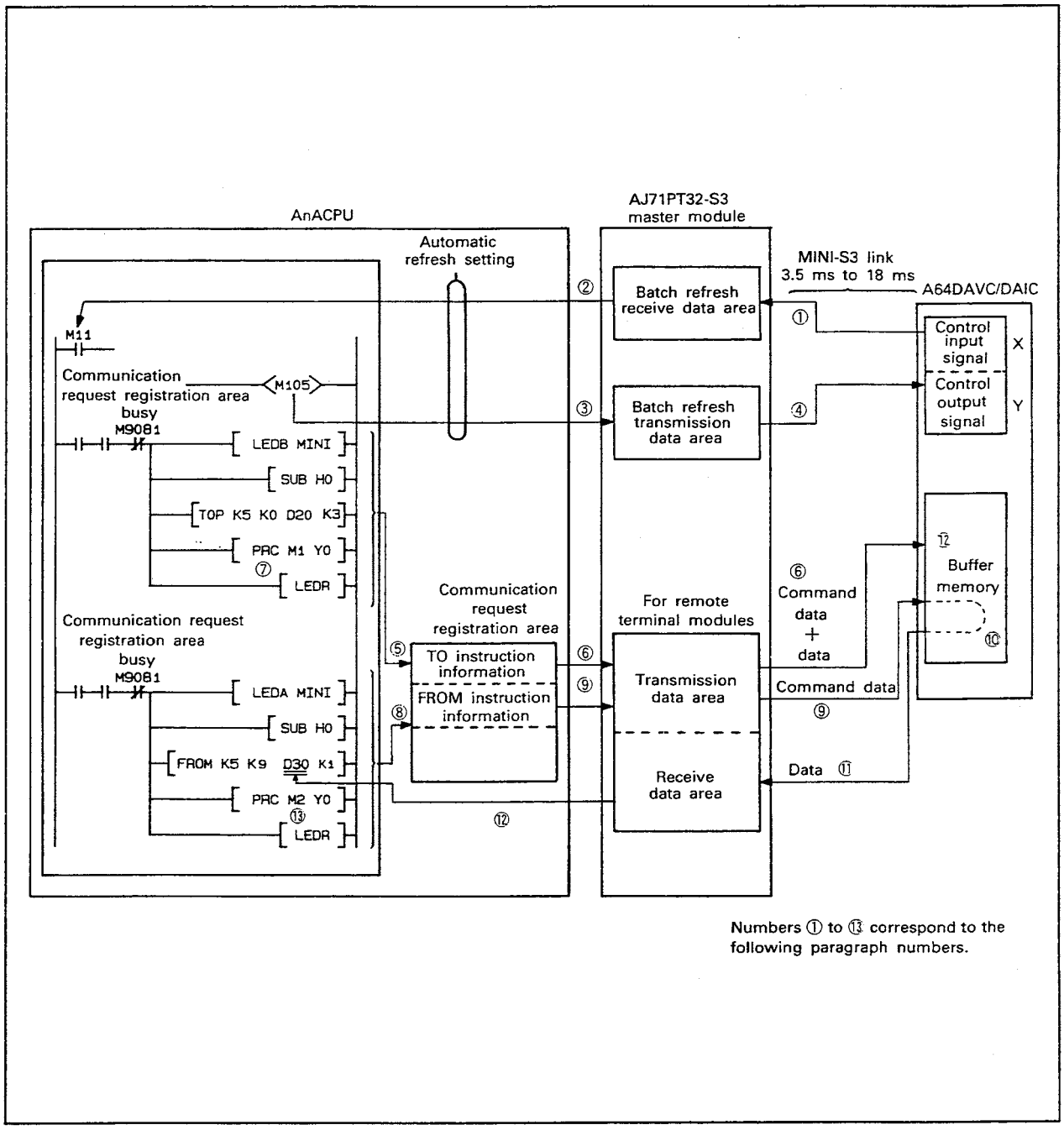


Fig. 4.1 Communication Procedures

(1) Communication processes of control input/output signals used for interlocking of the A64DAVC/DAIC and the AnACPU

① **Control input signals from the A64DAVC/DAIC are stored automatically in the batch refresh receive data area in the master module at 3.5 to 18 ms intervals.**

② Control input signals stored in the batch refresh receive data area are refreshed to the receive data storage devices as set with parameters.

③ The transmit data storage device ON/OFF information set by automatic refresh setting of parameters is automatically refreshed to the batch refresh transmission data area.

④ **Control output signals stored in the batch refresh transmission data area are transmitted to the A64DAVC/DAIC at 3.5 to 18 ms intervals.**

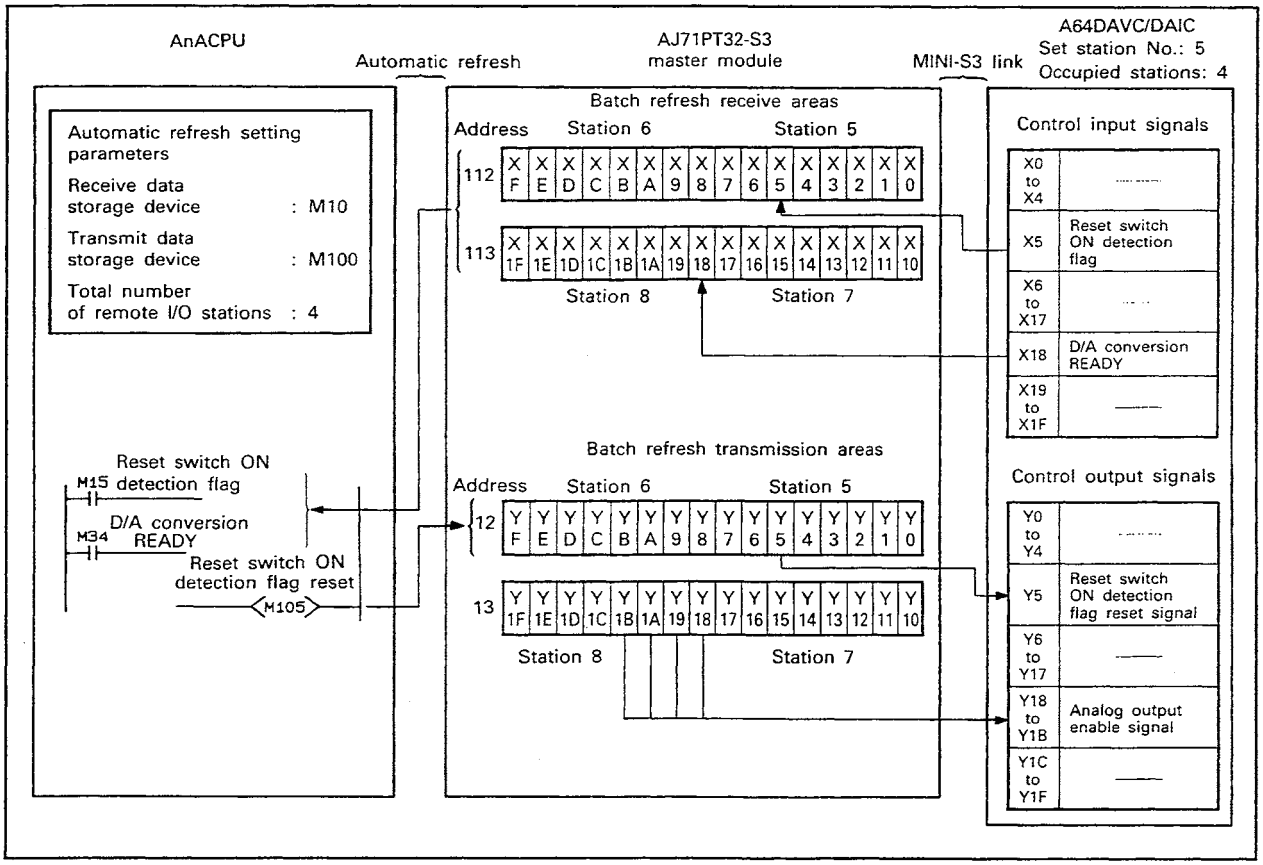


Fig. 4.2 Communication of Control I/O Signals

If automatic refresh is set, it is not necessary to use the FROM/TO instructions for data communication between the PLC CPU and the batch refresh transmission/receive areas of the master module.

POINT

For details of automatic refresh of the MINI-S3 link, read Section 3.6 "MELSECNET/MINI-S3 Automatic Refresh" of A2A(S1)/A3ACPU User's Manual (Control Functions).

(2) Writing data to the A64DAVC/DAIC buffer memory

⑤ By execution of the "LEDB MINI - TO" instruction (MINI-S3 dedicated instructions) of the sequence program, information such as master module I/O addresses, A64DAVC/DAIC station setting, buffer memory addresses and write instruction commands is stored in the communication request registration areas.

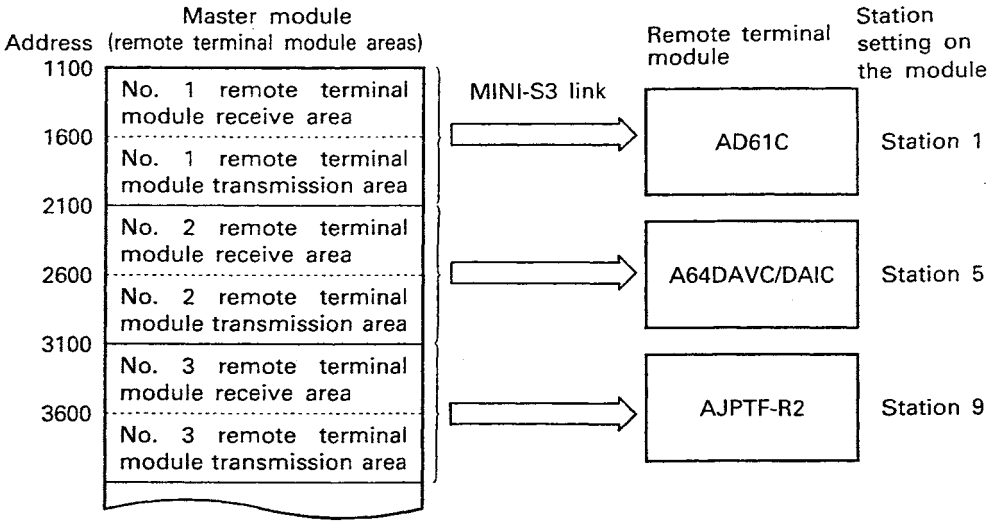
⑥ By execution of the PRC instruction, transmission data is written to the remote terminal module transmission data areas in the master module according to the TO instruction information stored in the communication request registration area. When the data write is completed, the data is transmitted to the A64DAVC/DAIC through the MINI-S3 link. This transmission is performed several times. (one word data per one time)

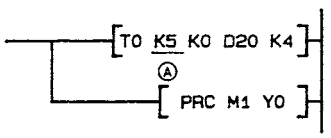
The remote terminal module areas correspond to the remote terminal modules connected to the MINI-S3 link as shown below.

When the initial data stored in the initial data ROM mounted to the master module is as shown right:

No. 1 remote terminal = Station 1
No. 2 remote terminal = Station 5
No. 3 remote terminal = Station 9

See Section 4.5.1 for details of the initial data.





If the program shown left is executed, 4 words of data beginning from D20 are written to the transmission areas of No. 2 remote terminal module which corresponds to Station 5 being set with (A).

⑦ When the transmission completion response of the A64DAVC/DAIC is received by the AnACPU via the receive data areas in the master module, the communication completion flag (device M1 in Fig. 4.1) designated by the PRC instruction turns ON for 1 scan. When communication is completed, the TO instruction information stored in the communication request registration area is cleared.

(3) Reading data from the A64DAVC/DAIC buffer memory

⑧ By execution of the "LEDA MINI to FROM" instruction (MINI-S3 dedicated instructions) of the sequence program, information such as master module I/O addresses, A64DAVC/DAIC station setting, buffer memory addresses and read instruction commands is stored in the communication request registration areas.

⑨ By execution of the PRC instruction, the FROM instruction information stored in the communication request registration area is written to the remote terminal module transmit data areas in the master module. When the information write is completed, the data is transmitted to the A64DAVC/DAIC through the MINI-S3 link. This transmission is performed several times. (one word data per one time)

⑩ When the A64DAVC/DAIC has received the FROM instruction information, it sends data stored in the buffer memory back to the master module according to the address data of the information. (one word data per one time)

⑪ Data received from the A64DAVC/DAIC is stored in the receive areas of remote terminal numbers corresponding to station setting of the A64DAVC/DAIC.

⑫ Data stored in the remote terminal module receive data areas is stored in the word devices designated by the FROM instruction.

⑬ After storing the data received from the A64DAVC/DAIC buffer memory in the designated devices, the AnACPU turns ON the communication completion flag (device M2 in Fig. 4.1) designated by the PRC instruction for 1 scan. When communication is completed, the FROM instruction information stored in the communication request registration area is cleared.

4.2.2 Processing time

(1) Data write time

Maximum processing time
= 2 scan time + tms × (Number of write data words + 7) + *1 40 ms

(2) Data read time

Maximum processing time
= 2 scan time + tms × (Number of read data words +8) + *1 40 ms

*1: Internal processing time of the A64DAVC/DAIC

"t" is the I/O refresh time and varies with the number and type of connected remote module stations.
The I/O refresh time is calculated as follows.

Mode	Mode Setting	I/O Refresh Time (msec)
Extension mode (48 points)	Automatic return enable (0)	t = 0.66 + (0.044 × R) + (0.25 × B) + (0.95 × T)
	Automatic return disable (1)	t = 0.54 + (0.058 × R) + (0.25 × B) + (0.95 × T)
	Communication stop at error detection (2)	t = 0.54 + (0.051 × R) + (0.25 × B) + (0.95 × T)

R : Total number of remote stations
B : Number of AJ35PTF-128DT modules
T : Number of remote terminal modules

4.3 I/O Signals Handled With the PLC CPU

4.3.1 I/O signals assigned to the A64DAVC/DAIC

Functions of the control input and output signals handled between the A64DAVC/DAIC and AnACPU are described in this section. Devices X refer to the input signals from the A64DAVC/DAIC to the AnACPU. Devices Y refer to the output signals from the AnACPU to the A64DAVC/DAIC.

Signal Direction: A64DAVC/DAIC → A2CCPU		Signal Direction: A2CCPU → A64DAVC/DAIC	
Device No.	**Description**	**Device No.**	**Description**
X(n+0) to X(n+4)	Unusable	Y(n+0) to Y(n+4)	Unusable
X(n+5)	Reset switch ON detection flag of the A64DAVC/DAIC module	Y(n+5)	Reset switch ON detection flag reset signal
X(n+6) to X(n+17)	Unusable	Y(n+6) to Y(n+17)	Unusable
X(n+18)	D/A conversion READY (1) Turns ON when D/A conversion is ready in the normal mode (other than the test mode) after the A64DAVC/DAIC was turned on or the PLC CPU was reset. (2) Turns OFF when mode is switched from normal to test. (3) Used for the interlock for reading and writing from the PLC CPU to the A64DAVC/DAIC.	Y(n+18)	Analog output enable signal for channel 1 *1
		Y(n+19)	Analog output enable signal for channel 2 *1
		Y(n+1A)	Analog output enable signal for channel 3 *1
		Y(n+1B)	Analog output enable signal for channel 4 *1
X(n+19) to X(n+1F)	Unusable	Y(n+1C) to Y(n+1F)	Unusable

Table 4.1 List of Input/output Signals

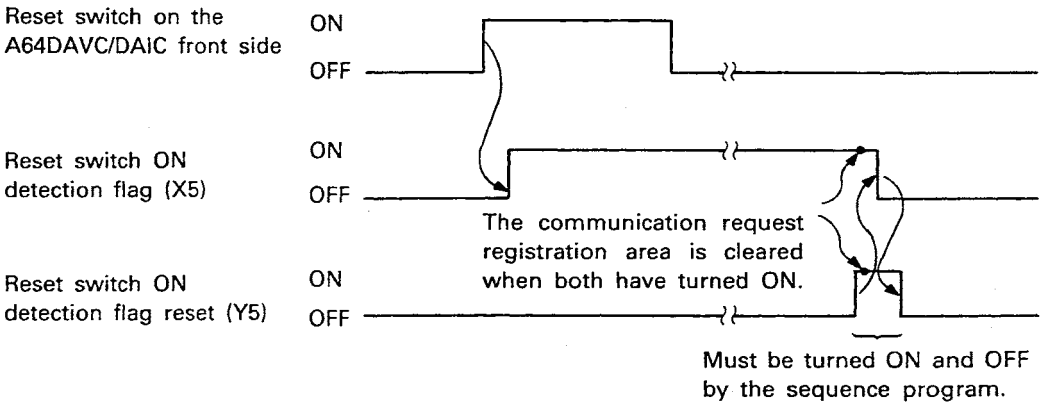
POINT

***1 Analog output enable signals ($Y_{(n+18)}$ to $Y_{(n+1B)}$) change in analog output condition between normal and test modes.**
(1) For analog output in normal mode, see Section 2.2.3 (3).
(2) In test mode, offset/gain values are output without regard to ON/OFF of the analog output enable signal of each channel.

IMPORTANT

Devices $Y_{(n+0)}$ to $Y_{(n+4)}$, $Y_{(n+6)}$ to $Y_{(n+17)}$ and $Y_{(n+1C)}$ to $Y_{(n+1F)}$ are unusable since they are used in the system.
If any of these devices are used (ON/OFF) in the sequence program, functions of the A64DAVC/DAIC are not guaranteed.

(1) Reset switch ON detection flag (X5) and reset switch ON detection flag reset signal (Y5)
Turns ON (latched) when the reset switch of the A64DAVC/DAIC is moved to reset.
When both the reset switch ON detection flag and the reset switch ON detection flag reset signal have turned ON, the FROM/TO instruction information, stored in the communication request registration area, of the corresponding remote terminal module is cleared.
To restart communication, turn ON the reset switch ON detection flag reset signal (Y5) with the sequence program.



POINT

(1) If the A64DAVC/DAIC is reset by moving the reset switch, it returns to the initial state. Start operation from the initial setting.
(2) Since X5 turns ON also after the power is turned on, be sure to turn ON Y5 and OFF X5 at the initial stage. And then, execute program for the A64DAVC/DAIC.

4.3.2 I/O signals of the AJ71PT32-S3

Device No.	Signal Name		Device No.	Signal Name	
X (n + 0)	Transmission completion signal	For remote terminal module No. 1	Y (n + 0)	Transmission request signal	For remote terminal module No. 1
X (n + 1)	Read request signal		Y (n + 1)	Read completion signal	
X (n + 2)	Transmission completion signal	For remote terminal module No. 2	Y (n + 2)	Transmission request signal	For remote terminal module No. 2
X (n + 3)	Read request signal		Y (n + 3)	Read completion signal	
X (n + 4)	Transmission completion signal	For remote terminal module No. 3	Y (n + 4)	Transmission request signal	For remote terminal module No. 3
X (n + 5)	Read request signal		Y (n + 5)	Read completion signal	
X (n + 6)	Transmission completion signal	For remote terminal module No. 4	Y (n + 6)	Transmission request signal	For remote terminal module No. 4
X (n + 7)	Read request signal		Y (n + 7)	Read completion signal	
X (n + 8)	Transmission completion signal	For remote terminal module No. 5	Y (n + 8)	Transmission request signal	For remote terminal module No. 5
X (n + 9)	Read request signal		Y (n + 9)	Read completion signal	
X (n + A)	Transmission completion signal	For remote terminal module No. 6	Y (n + A)	Transmission request signal	For remote terminal module No. 6
X (n + B)	Read request signal		Y (n + B)	Read completion signal	
X (n + C)	Transmission completion signal	For remote terminal module No. 7	Y (n + C)	Transmission request signal	For remote terminal module No. 7
X (n + D)	Read request signal		Y (n + D)	Read completion signal	
X (n + E)	Transmission completion signal	For remote terminal module No. 8	Y (n + E)	Transmission request signal	For remote terminal module No. 8
X (n + F)	Read request signal		Y (n + F)	Read completion signal	
X (n + 10)	Transmission completion signal	For remote terminal module No. 9	Y (n + 10)	Transmission request signal	For remote terminal module No. 9
X (n + 11)	Read request signal		Y (n + 11)	Read completion signal	
X (n + 12)	Transmission completion signal	For remote terminal module No. 10	Y (n + 12)	Transmission request signal	For remote terminal module No. 10
X (n + 13)	Read request signal		Y (n + 13)	Read completion signal	
X (n + 14)	Transmission completion signal	For remote terminal module No. 11	Y (n + 14)	Transmission request signal	For remote terminal module No. 11
X (n + 15)	Read request signal		Y (n + 15)	Read completion signal	
X (n + 16)	Transmission completion signal	For remote terminal module No. 12	Y (n + 16)	Transmission request signal	For remote terminal module No. 12
X (n + 17)	Read request signal		Y (n + 17)	Read completion signal	
X (n + 18)	Transmission completion signal	For remote terminal module No. 13	Y (n + 18)	Transmission request signal	For remote terminal module No. 13
X (n + 19)	Read request signal		Y (n + 19)	Read completion signal	
X (n + 1A)	Transmission completion signal	For remote terminal module No. 14	Y (n + 1A)	Transmission request signal	For remote terminal module No. 14
X (n + 1B)	Read request signal		Y (n + 1B)	Read completion signal	
X (n + 1C)	Unusable		Y (n + 1C)	Unusable	
X (n + 1D)			Y (n + 1D)		
X (n + 1E)			Y (n + 1E)		
X (n + 1F)			Y (n + 1F)		
X (n + 20)	Hardware error		Y (n + 20)		
X (n + 21)	MINI-S3 link communicating		Y (n + 21)		
X (n + 22)	Unusable		Y (n + 22)		
X (n + 23)	Receive data clear completion		Y (n + 23)	Receive data clear request	
X (n + 24)	Remote terminal module error detection		Y (n + 24)	Remote terminal module error detection reset	
X (n + 25)	Test mode		Y (n + 25)	Unusable	
X (n + 26)	MINI-S3 link error detection		Y (n + 26)		
X (n + 27)	MINI-S3 link communication error		Y (n + 27)		
X (n + 28)	ROM error		Y (n + 28)	MINI-S3 link communication start	
X (n + 29)	Unusable		Y (n + 29)	Unusable	
X (n + 2A)			Y (n + 2A)	FROM/TO instruction response designation	
X (n + 2B)			Y (n + 2B)	Faulty station data clear designation	
X (n + 2C)			Y (n + 2C)	Unusable	
X (n + 2D)			Y (n + 2D)	Error reset	
X (n + 2E)			Y (n + 2E)	Unusable	
X (n + 2F)			Y (n + 2F)		

Table 4.2 List of I/O Signals

"n" specifies value of the head I/O address of the AJ71PT32-S3.
Example) When the I/O address of the AJ71PT32-S3 is between X/Y20 and X/Y4F: $X_{(n+0)}$ to $X_{(n+2F)}$ = X20 to X4F
$Y_{(n+0)}$ to $Y_{(n+2F)}$ = Y20 to Y4F

REMARK

For details of functions and purposes of control I/O signals, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

4.4 Assignment of Buffer Memory

Assignment of the A64DAVC/DAIC buffer memory (without battery backup) is shown below.

Address		Default	
0	CH1 Digital value setting area	0	Read/write from the PC CPU is possible.
1	CH2 Digital value setting area	0	
2	CH3 Digital value setting area	0	
3	CH4 Digital value setting area	0	
4	CH1 Analog output enable/disable setting area	0 (Enable)	
5	CH2 Analog output enable/disable setting area	0 (Enable)	
6	CH3 Analog output enable/disable setting area	0 (Enable)	
7	CH4 Analog output enable/disable setting area	0 (Enable)	
8	Digital resolution setting area	1 (1/4000)	
9	Error code storage area	0	

*All 16-bit data.

POINT

When the A64DAVC/DAIC has detected an error, the error code is stored in address 9, and the RUN LED flickers.

4.4.1 Contents and data configuration of the buffer memory

Contents of memory items and data configuration of the buffer memory are as follows.

(1) Digital value setting areas for CH1 to CH4 (Addresses 0 to 3)
  (a) Digital values for D/A conversion are written to these areas from the A2CCPU.
  (b) Setting ranges are as shown below.

Module	Digital Value Resolution Setting	Setting Range	Digital Value for D/A Conversion when Values Outside the Specified Ranges are Set.	
A64DAVC	1/4000	−4096 to 4095	−4097 and below: −4096	4096 and above: 4095
	1/8000	−8192 to 8191	−8193 and below: −8192	8192 and above: 8191
	1/12000	−12288 to 12287	−12289 and below: −12288	12288 and above: 12287
A64DAIC	1/4000	0 to 4095	−1 and below: 0	4096 and above: 4095
	1/8000	0 to 8191	−1 and below: 0	8192 and above: 8191
	1/12000	0 to 12287	−1 and below: 0	12288 and above: 12287

  (c) In the cases below, digital values for all channels for D/A conversion turn to 0.
    1) When the D/A conversion READY (X18) is turned ON after the A64DAVC/DAIC was powered on.
    2) When the D/A conversion READY (X18) is turned ON after the A64DAVC/DAIC module was reset.

(2) Analog output enable/disable setting areas for CH1 to CH4 (Addresses 4 to 7)
  (a) Used to set analog output enable/disable after D/A conversion.
  (b) Analog output enable/disable setting is done by writing 1 or 0 to corresponding setting area.
    • 0: Enable
    • 1: Disable

POINT

If a value other than 1 and 0 is written, analog output is processed according to the set data before writing, and the error code is stored in the error code storage area (address 9).

  (c) In the cases below, all channels are set for analog output enable. (Default)
    1) When the A64DAVC/DAIC is powered on.
    2) When the A64DAVC/DAIC module was reset.

(3) Digital value resolution setting area (Address 8)
  (a) Used to set digital value resolution with respect to analog output voltage range.
    Resolution setting is common to all channels.
  (b) Setting values are 1/4000, 1/8000 and 1/12000.
    Values 1, 2 and 3 are used with 1/4000 resolution as the standard value.

Example) To set resolution at 1/8000.

Write "2" in address 8.

1/8000 = 1/4000 (standard) × 2

1/8000 resolution indicates the absolute value range of analog output voltage (0 to ±10 V).

−10 to 0 V, 0 to 10 V (1/8000) (1/8000) ⇨ −10 to 0 to 10 V (1/16000)

POINT

If a value other than 1, 2 and 3 is written, digital value resolution is processed according to the set data before writing or to default, and the error code is stored in the error code storage area (address 9).

  (c) In the cases below, digital value resolution is set at "1" (1/4000). (Default)
    1) When the A64DAVC/DAIC is powered on.
    2) When the A64DAVC/DAIC module was reset.

(4) Error code storage area (Address 9)

(a) When data is read from the PLC CPU, the A64DAVC/DAIC performs data range check and read/write area access checks once respectively. Any value outside the range is stored as error codes in 16-bit binary.
For details of error codes, see Section 7.1.

(b) When several error codes have occurred, the first error code detected by the A64DAVC/DAIC is stored, and the rest are not stored.

(c) To reset an error code, write 0 from the PLC CPU. If an error code is reset, the write data error code is set to "0" and the RUN LED of the A64DAVC/DAIC changes from flickering to illuminating.

4.4.2 Contents and configuration of the AJ71PT32-S3 buffer memory

The AJ71PT32-S3 is provided with a buffer memory (without battery backup) for data communication with the PLC CPU. Use the FROM/TO instructions to read and write data from to the buffer memory.

(1) Assignment of the buffer memory

Address (decimal)			Content	Read/write by PLC CPU
0	(Unused)		—	Read/write enable
1	Retry count		Sets the number of retries when communication error has occurred.	
	(Unused)		—	
4	Line error check		Checks location of line error.	
	(Unused)		—	
10 to 41	Batch refresh transmission data		Writes data to be output to the batch refresh type remote I/O module.	
	(Unused)		—	—
70 to 77	Remote module card information		Stores type identification of each remote module being connected.	Read only
	(Unused)		—	—
90 to 93	Accumulated faulty station detection		Stores faulty remote station numbers. (Detected state is retained until reset.)	Read/write enable
	(Unused)		—	—
100 to 103	Faulty station detection		Stores faulty remote station numbers. (Update state is retained.)	Read only
	(Unused)		—	
107	Communication error code		Stores the cause of the MINI-S3 link communication error signal ON.	
108	Error detection code		Stores accumulated count of the MINI-S3 link error detection ON.	
	(Unused)		—	
110 to 141	Batch refresh receive data		Stores the input data from the batch refresh type remote I/O modules.	
	(Unused)		—	
160	Line error retry counter		Stores the number of retries when communication with all remote modules fails due to line error.	
161 to 192	Retry counter		Stores the number of retries executed to faulty stations.	
	(Unused)		—	
195	Remote terminal module faulty station	(*1)	Stores the station number when a remote terminal module has caused an error.	
196 to 209	Remote terminal module error code	(*1)	Stores the cause of the remote terminal module error detection signal X(n+24) ON.	
	(Unused)		—	—
250 to 282	Partial refresh station set data	(*2)	Writes the station number and digit designation (number of time of division) of the partial refresh type remote I/O module.	Read/write enable
	(Unused)		—	
300 to 363	Partial refresh transmission data		Writes data to be output to the partial refresh type remote I/O module.	
	(Unused)		—	
598	Partial refresh accumulated input error detection		Stores the input faulty station number of the partial refresh type remote I/O module input data. (Detected state is retained until reset.)	
599	Partial refresh input error detection		Stores the input faulty station number of the partial refresh type remote I/O module input data. (Update state of communication is stored.)	
600 to 663	Partial refresh receive data		Stores input data of the partial refresh type remote I/O module.	Read only

Address (decimal)			Content	Read/write by PLC CPU
858	Receive data clear designation		Sets the AJ35PTF-R2 station that clears receive data by the receive data clear request signal Y(n+23).	Read/write enable
859	Receive data clear range designation		Designates the receive buffer that clears receive data by the receive data clear request signal Y(n+23).	
860 to 929	No-protocol mode parameter		Sets the parameters when the AJ35PTF-R2 is used in the no-protocol mode.	
930 to 1099	(Unused)		---	---
	(*1) Channel 0	(*1) Channel 1		
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8	Areas to which transmission data to remote terminal modules is written or to store data received from remote terminal modules.	Read/write enable
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9		
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10		
4100 to 5099	Communication area for remote terminal No. 4	Communication area for remote terminal No. 11		
5100 to 6099	Communication area for remote terminal No. 5	Communication area for remote terminal No. 12		
6100 to 7099	Communication area for remote terminal No. 6	Communication area for remote terminal No. 13		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14		

POINT

(1) Channels specified with *1 are used for executing read/write at areas of addresses 1100 to 8099 and are automatically switched according to the remote terminal module station number as designated by the MINI-S3 dedicated instructions.

(2) The buffer memory is all cleard (0 is stored.) at power on or when the PLC CPU is reset. However, retry count (adress 1) and no-protocol mode parameters (adresses 860 to 929) are set at defaults.

(3) Do not write data from the PLC CPU to read only areas.

(4) Unused areas are used by the system of the master module.

(5) Data in the buffer memory can be read continuously including unused areas. For example, data of accumulated faulty stations detection (addresses 90 to 93) and faulty station detection (addresses 100 to 103) can be read by a single FROM instruction.

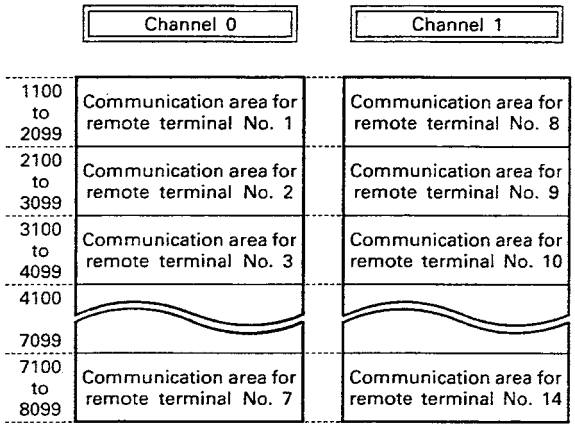
REMARK

For details of contents at each address and data configuration of the buffer memory, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

(2) Remote terminal communication areas (addresses 1100 to 8099)

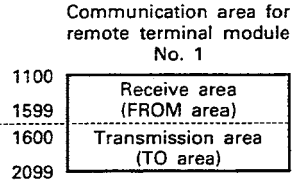
(a) Areas for data communication with remote terminal modules.

(b) The communication areas are assigned to two channels. Channel 0 is assigned to remote terminal modules No. 1 to No. 7, and channel 1 is assigned to remote terminal modules No. 8 to No. 14.
Channels are automatically switched according to the remote terminal module station number as designated by the MINI-S3 dedicated instructions.



The remote terminal module number refers to the number assigned to each remote terminal module set in the initial data ROM of the master module.
Data read/write is executed for areas which correspond to the module numbers assigned to each remote terminal module.

(c) Each communication area consists of a transmission area and a receive area. Capacity of each area at power on is 500 words.

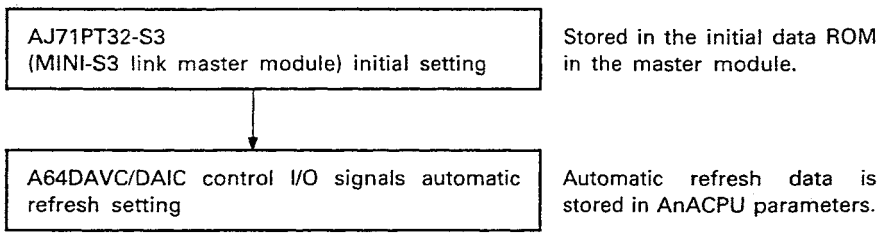


The transmission area sets data to be transmitted to remote terminal modules.
The receive area stores data received from remote terminal modules.

(d) Capacity of the transmission and receive areas can be changed by the initial data setting of the master module. (Note that the total capacity of the two areas must not exceed 1000 words.)
Example) Receive area: 200 words, Transmission area: 800 words

4.5 Contents of Initial Setting

The contents of initial setting when the A64DAVC/DAIC is used as a remote terminal module employing the MELSECNET/MINI-S3 dedicated instructions (hereinafter referred to as the MINI-S3 dedicated instructions) for the AnACPU are described.



4.5.1 Initial setting of the AJ71PT32-S3

Use the SW□GP-MINIP system disk to set initial data and to store it in the initial data ROM.
The initial data ROM is inserted to the ROM socket of the AJ71PT32-S3.
Contents of initial data setting are mentioned below.

- Total number of remote stations: Set the total number of occupied stations of each module connected to the MINI-S3 link.
  Example) AJ35PTF-32A (remote I/O module) 4 stations
  A64DAVC/DAIC (remote terminal module) 4 stations
  AJ35PTF-24T (remote I/O module) 4 stations
  Total: 12 stations

- Station number of each remote terminal number: Set the station numbers set for modules which correspond to remote terminal modules No. 1 to No. 14.
  Example) AJ35PTF-32A 1 stations
  A64DAVC/DAIC 5 stations ← Remote terminal module
  AJ35PTF-24T 9 stations
  Remote terminal No. 1=5 stations

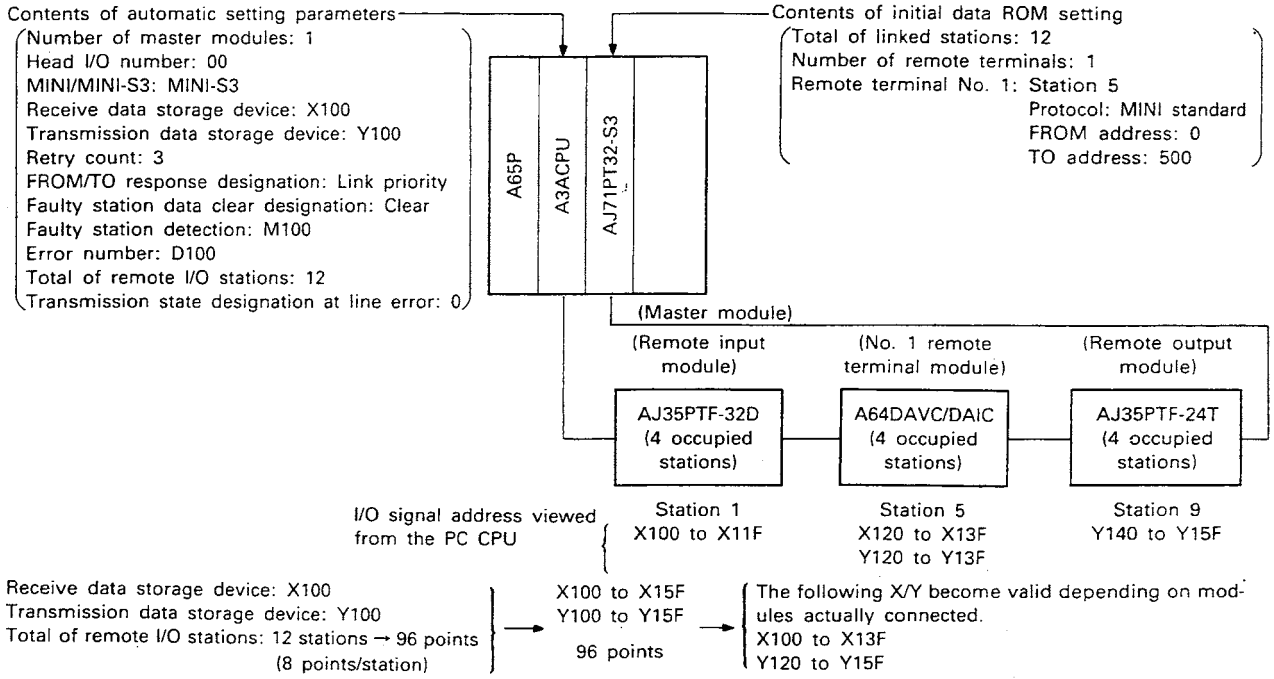
- Protocol: Set the protocol used for communications with the A64DAVC/DAIC.
  Use the MINI standard protocol.

- Remote terminal FROM/TO area setting: Set the capacity for the FROM area and the TO area as explained in Section 4.4.2 (2).
  Default is 500 words for each of the FROM area and the TO area.

For details of setting procedures, refer to SW□GP-MINIP Operating Manual.

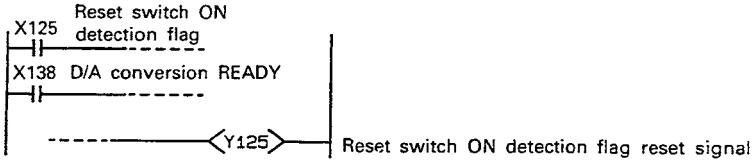
4.5.2 A64DAVC/DAIC control I/O signals automatic refresh setting

For details of contents of automatic refresh setting, refer to Section 3.6 MELSECNET/MINI(S3) Automatic Refresh of the A2A(S1)/A3ACPU User's Manual (Control Functions).
The following is an example of automatic refresh setting.



In the case of the system configuration and setting shown above, the A64DAVC/DAIC control I/O signals correspond to the device numbers shown below. Devices assigned to control input signals turn ON/OFF automatically as the A64DAVC/DAIC state changes. When devices assigned to control output signals are turned ON/OFF by the sequence program, the device states are written to the batch refresh transmission areas of the master module and then transmitted to the A64DAVC/DAIC.

AnACPU device	A64DAVC/DAIC control I/O signal
X125 ← X5	Reset switch ON detection flag
X138 ← X18	D/A conversion READY
X125 → Y5	Reset switch ON detection flag reset signal



4.6 Programming

This section describes the programming procedures when the MINI-S3 dedicated instructions of the AnACPU are used for data communication with the A64DAVC/DAIC connected to the MINI-S3 link.

4.6.1 Writing data to the A64DAVC/DAIC

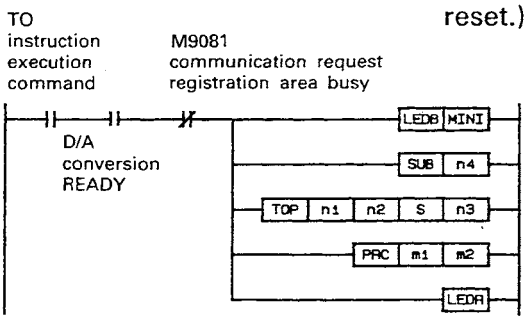
Instructions from LEDB MINI to LEDR are handled as one block of instructions in the sequence program to write data to the buffer memory of designated remote terminal module.
Items of the buffer memory and procedures of writing to the A64DAVC/DAIC are described below.

(a) Digital value for each channel

(b) Analog output enable/disable setting for each channel

(c) Digital value resolution setting

(d) Error code clear ("0" is written from the AnACPU at error code reset.)



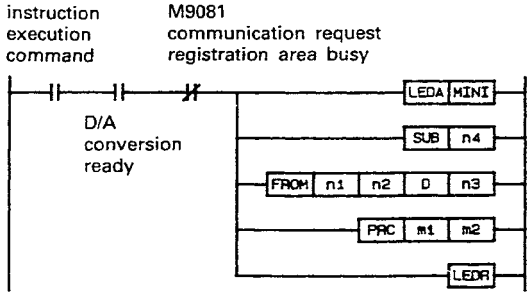
n1	Head station number of remote terminal module
n2	Head address of the buffer memory for writing
S	Head number of write data or of device which stores write data
n3	Number of write data
n4	Higher 2 digits of head I/O number assigned to AJ71PT32-S3
m1	Device number to be turned ON for 1 scan when execution of the TO instruction is completed
m2	Dummy device number

For details of instructions, refer to the A2A(S1)/A3ACPU Programming Manual (Dedicated Instructions).

4.6.2 Reading data from the A64DAVC/DAIC

Instructions from LEDA MINI to LEDR are handled as one block of instructions in the sequence program to read data from the buffer memory of designated remote terminal module.
Items of the buffer memory and procedures of reading from the A64DAVC/DAIC are described below.

(a) Write data error code

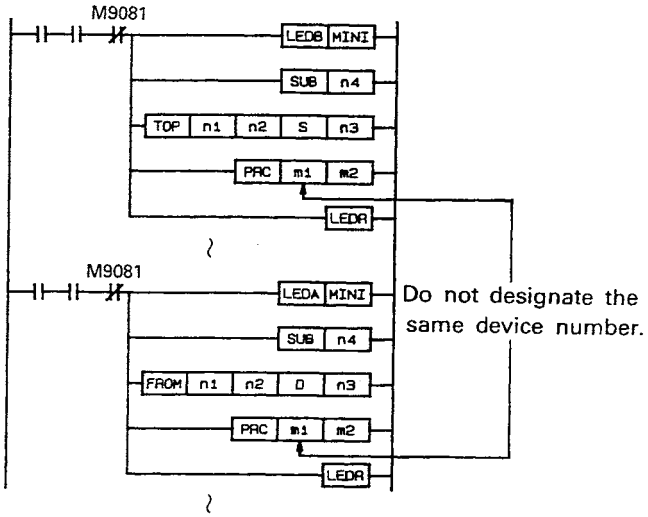


n1	Head station number of remote terminal module
n2	Head address of the buffer memory for reading
D	Head number of the device which stores read data
n3	Number of read data
n4	Head I/O number assigned to AJ71PT32-S3
m1	Device number to be turned ON for 1 scan when execution of the FROM instruction is completed
m2	Dummy device number

For details of instructions, refer to the A2A(S1)/A3ACPU Programming Manual (Dedicated Instructions).

4.6.3 Cautions on programming

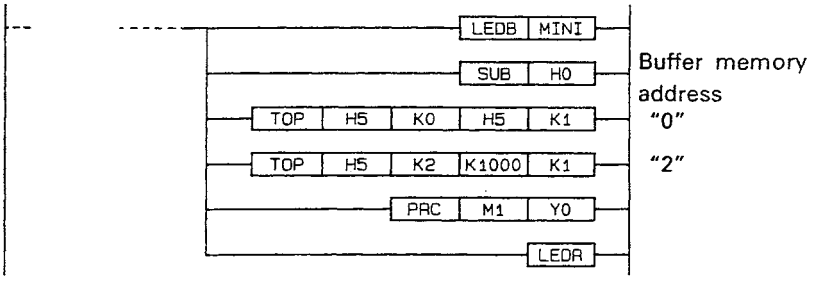
(1) It is necessary to provide the PRC instruction to the step immediately following the FROM/TO instruction. Use care not to designate same devices for "m1" of the PRC instruction and for "m1" of the PRC instruction provided to other step.



(2) The communication request registration areas can store a maximum of 32 FROM/TO instructions. If the 33rd FROM/TO instruction is executed, an operation error occurs.
Provide an interlock with M9081 and D9081 so that the FROM/TO instruction may not be executed when the communication request registration areas have become full.
M9081 and D9081 are described below.

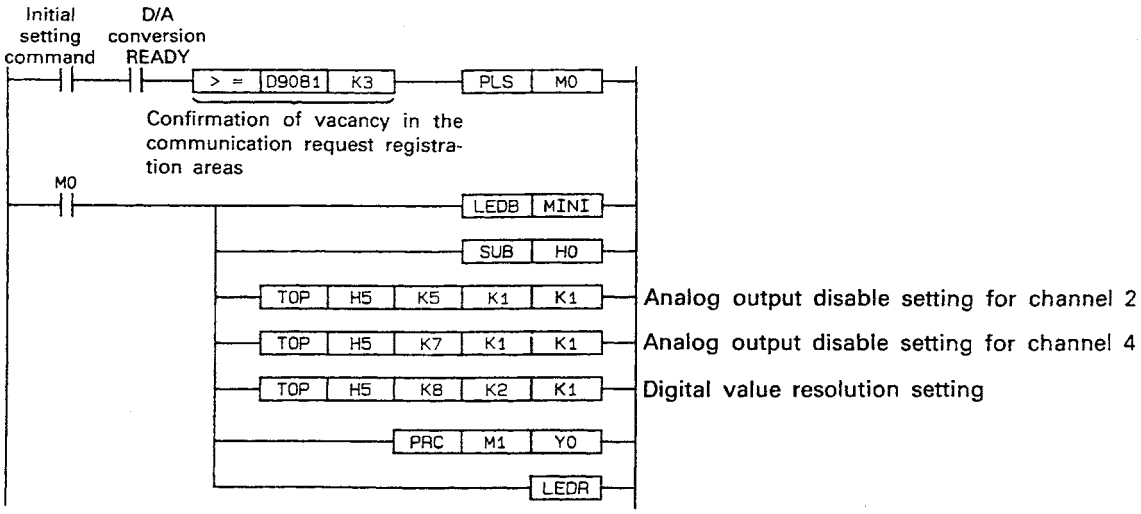
Number	Contents	Details
M9081	OFF: Communication request registration area has a vacancy. ON: Communication request registration areas are full.	There are 32 communication request registration areas for remote terminals. Turns ON when all areas become full.
D9081	The number of vacant areas of the communication request registration area for remote terminals.	The number of vacant areas of the communication request registration area is stored.

When data is written to two or more addresses in the buffer memory of the A64DAVC/DAIC, a single TO instruction can execute data write if the addresses are continuous. If the addresses are not continuous, it is necessary to execute the TO instruction at two or more points. (see below) In this case, the TO instruction information is stored in the communication request registration areas in plural.

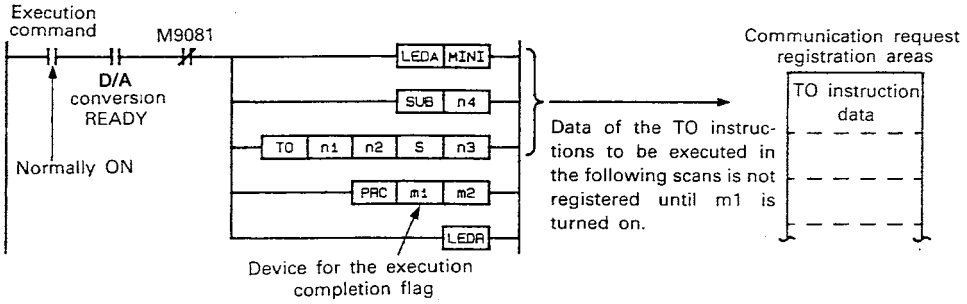


If an attempt is made to store the TO instruction information which is larger than the number of vacant areas of communication request registration areas, an error occurs and the CPU stops operation. To prevent this, it is necessary to provide a condition to allow confirmation that the vacancy in the communication request registration areas is larger than the number of TO instruction information. The programming example shown below describes the case when the TO instruction is executed after confirming the vacancy in the communication request registration areas.

Example) Initial setting program to the A64DAVC/DAIC
(Channels 2 and 4 are set for analog output disable. (Addresses 5 and 7)
Digital value resolution is set at 2 (1/8000).

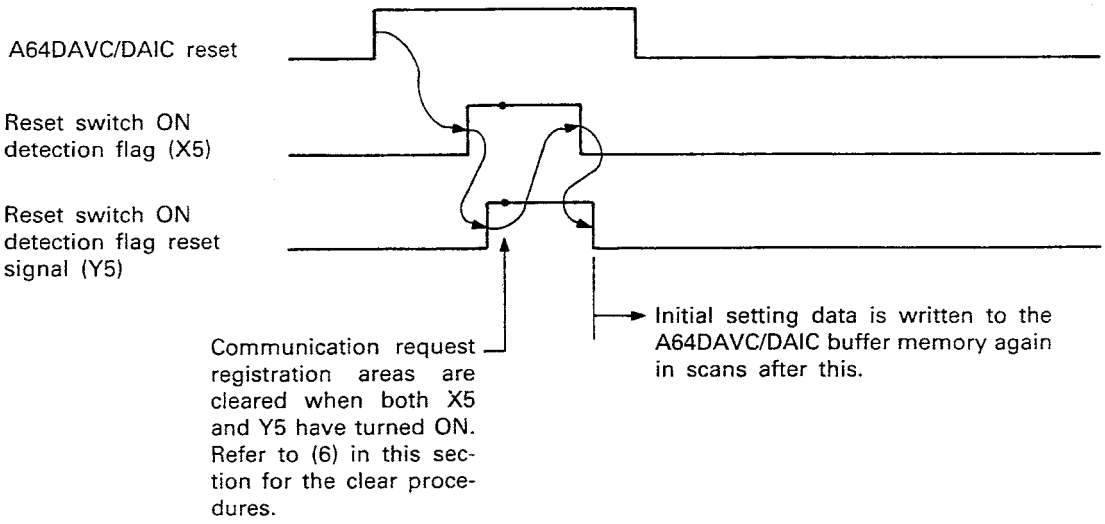


(3) When a TO instruction is being executed with the TO instruction execution command set for normally ON, the next TO instruction data will not be registered to the communication request registration areas until processing of the TO instruction being executed is completed and the execution completion flag specified by the PRC instruction is set.
It is not necessary to provide interlock that enables execution of the TO instruction after the execution completion flag is set.

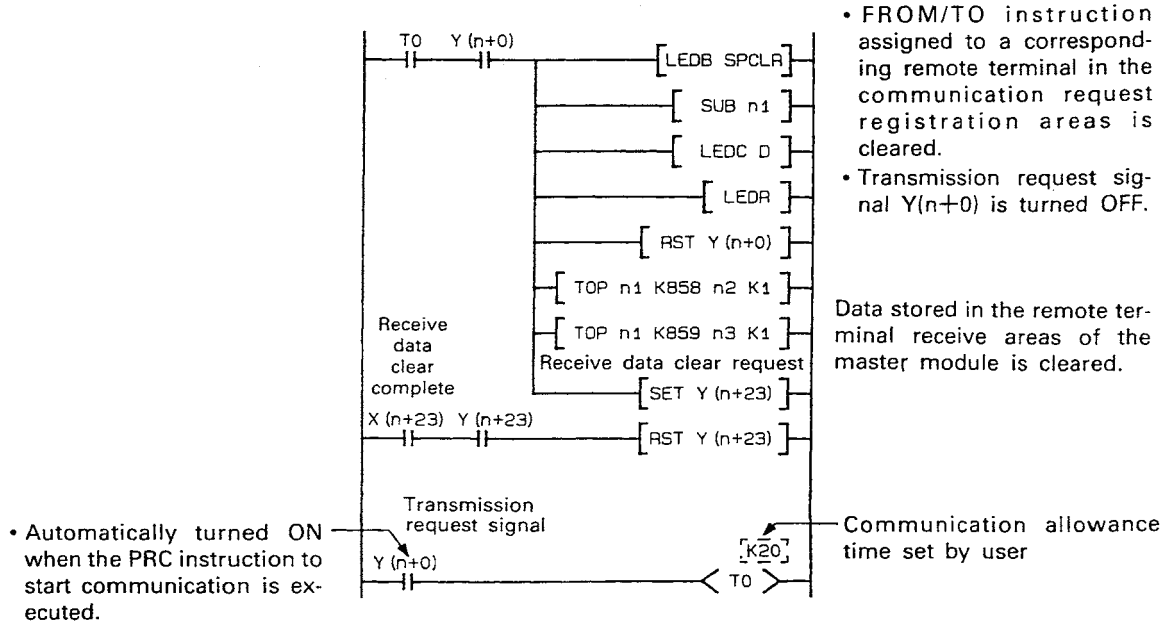


(4) For communication with the remote terminal modules linked to the AJ71PT32-S3, turn ON the AJ71PT32-S3 communication start signal Y(n+28) always before execution of each instruction. If the communication start signal has not turned ON, communication processings are not possible.
Though the MINI-S3 instruction is executed when the communication start signal is OFF, no error will occur. But, bit devices designated with m_1 of PRC m_1 m_2 does not turn ON.

(5) When the reset switch on the front of the A64DAVC/DAIC is moved to reset, the A64DAVC/DAIC returns to the initial state and performs D/A conversion with defaults.
Set the sequence program to continuously monitor the reset switch ON detection flag (X5) and, when the flag has turned ON, to clear the communication request registration areas and to write initial setting data again to the A64DAVC/DAIC. (when executed with other than defaults)



(6) If a communication completion response signal to the transmission executed to the A64DAVC/DAIC is not sent back, the CPU module is set in the state waiting for the communication completion signal infinitely unless the CPU module is reset. To prevent the infinite completion wait state, provide a monitoring timer to clear corresponding FROM/TO instruction information which is assigned to a corresponding remote terminal and stored in the communication request registration areas when the timer has timed out.

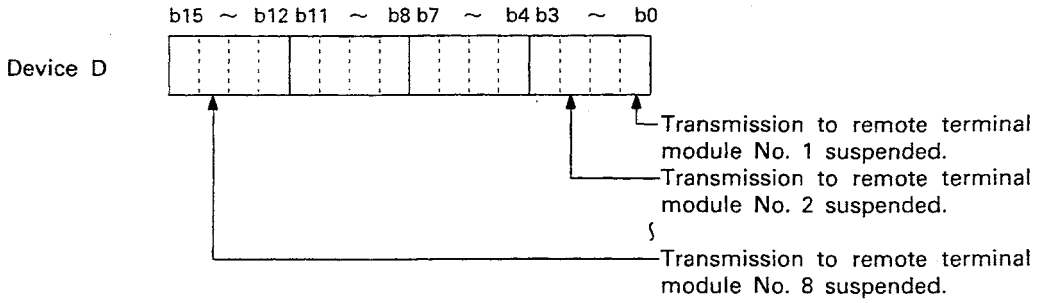


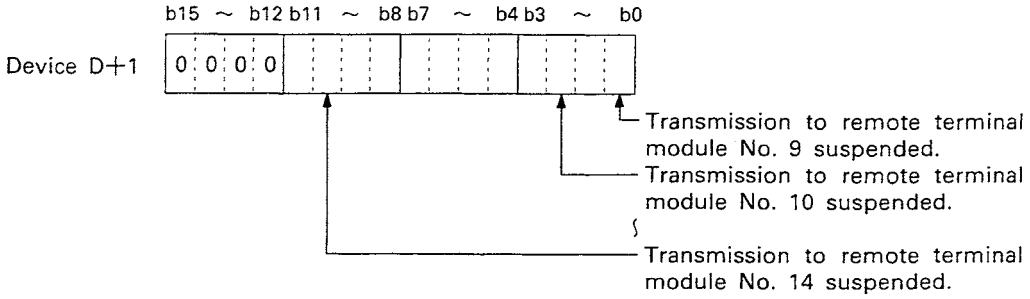
X(n+23), Y(n+0) and Y(n+23) are control I/O signals for the AJ71PT32-S3. See Section 4.3.2 for details.

Contents of n_1, n_2, n_3 and D designated by each instruction are as described below.

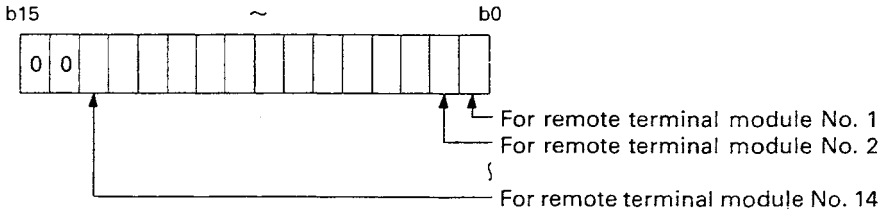
n_1: Higher 2 digits of head I/O number assigned to AJ35PT32-S3
Example) "12_H" when assigned to X/Y120 to 13F.

D : Data when the bit that corresponds to a processing to be suspended is set for "1".





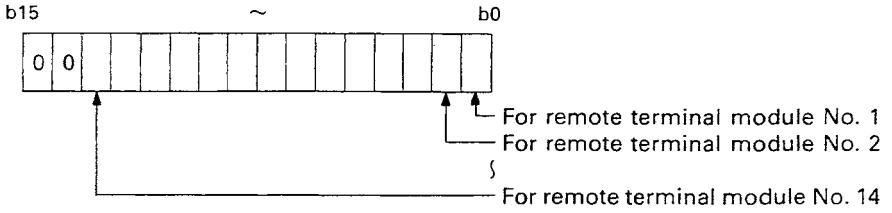
n_2: Receive buffer clear/no clear setting for each remote terminal number



0: No clear
1: Clear

Contents of setting are written to address 858 in the AJ71PT32-S3 buffer memory.

n_3: Clear execution range setting for each remote terminal number



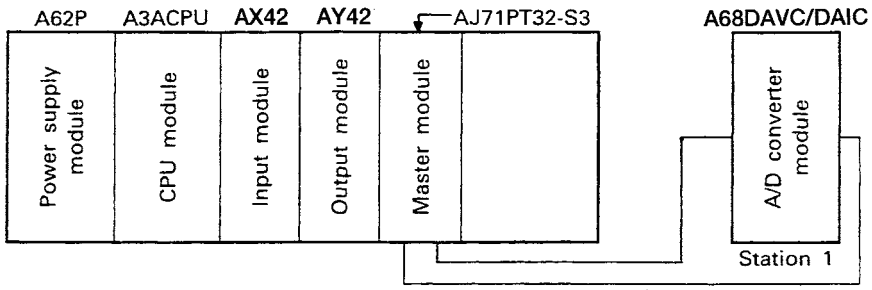
0: Only the remote terminal receive areas of the master module are cleared.
1: The remote terminal receive areas of the master module and the A64DAVC/DAIC receive buffer are cleared.

Contents of setting are written to address 859 in the AJ71PT32-S3 buffer memory.

(7) When automatic refresh is being set, the remote terminal module error detection $X_{(n+24)}$ of control I/O signals assigned to AJ71PT32-S3 turns ON for 1 scan after error detection.

4.6.4 Program example

The program example shown in this section writes the value (0 to 8000) set by the digital switch to channel 1 of the A64DAVC/DAIC in the following system configuration.
The resolution of the digital value is assumed to be 1/8000 and channels 2 to 4 to be disabled for analog output.



1) A3ACPU's automatic refresh settings. See Section 4.5.2.

Number of master modules: 1
Head I/O number: 80H
MINI/MINI-S3: MINI-S3
Device for storing receive data: B000
Device for storing transmission data: B100
Number of retries: 7
FROM/TO response setting: Priority given to link
Faulty station data clear setting: Clear
Faulty station detection: D5000
Error number: D6000
Total number of remote I/O stations: 4
Line error-time transmission status setting: 0

2) Master module's initial data ROM settings

Total number of link stations: 4
Number of remote terminals: 1
No. 1 remote terminal: Station 1
Protocol - MINI-standard
FROM address - 0
TO address - 500

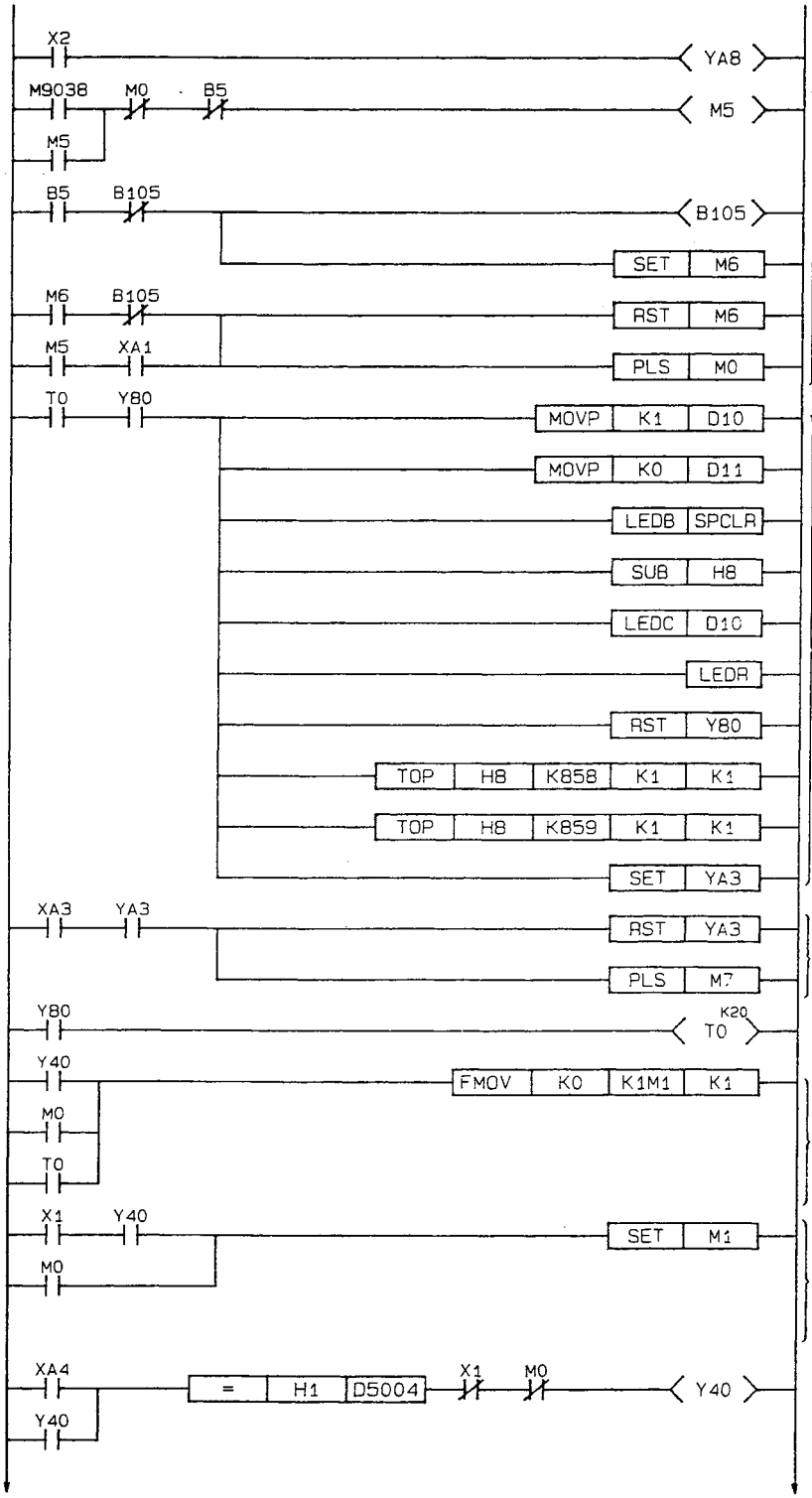
3) I/O numbers assigned to control I/O signals by CPU (by automatic refresh setting)

Device for storing receive data: B000 B000 to B01F = X0 to X1F
Device for storing transmission data: B100 ⇨ B100 to B11F = Y0 to Y1F
Total number of remote I/O stations : 4 to 32 (8 points per station)

I/O numbers assigned to A64DAVC/DAIC by CPU — A64DAVC/DAIC's I/O numbers

4) Program example

- Switching "on" X2 (MINI-S3 link communication start command) of the input module starts MINI-S3 link.
- Starting the MINI-S3 link communication enables channel 1 for analog output and switching "on" X0 (digital value setting command) of the input module writes the values of X10 to X1F (digital value setting, BCD 4 digits) to the A64DAVC/DAIC.
- Any digital value setting greater than 8000 switches "on" Y41 of the output module and is displayed by an external device.
- Detection of a communication error with the remote terminal unit switches "on" Y40 to stop all processings.
- Switching "on" X1 (communication error detection flag reset command) clears all the error status area and flags.
- Resetting the A64DAVC/DAIC stops all processings.
- Switching "on" B5 (reset "on" detection flag) clears all.



Switches on MINI-S3 link communication start.

Switches on M0 when CPU module reset or A64DAVC/DAIC hardware reset is performed.

Performs the following processings when communication response monitoring time-out occurs:

(1) Clears FROM/TO instruction information registered in AnACPU's communication request registration area.

(2) Switches off Y80 (transmission request signal to No. 1 remote terminal unit).

(3) Specifies clearing of master module's receive area for No. 1 remote terminal unit and sets receive data clear request signal (YA3).

Switches on M7 on receive data clear completion (XA3) and resets receive data clear request (YA3).

Communication response monitoring time is set by user.

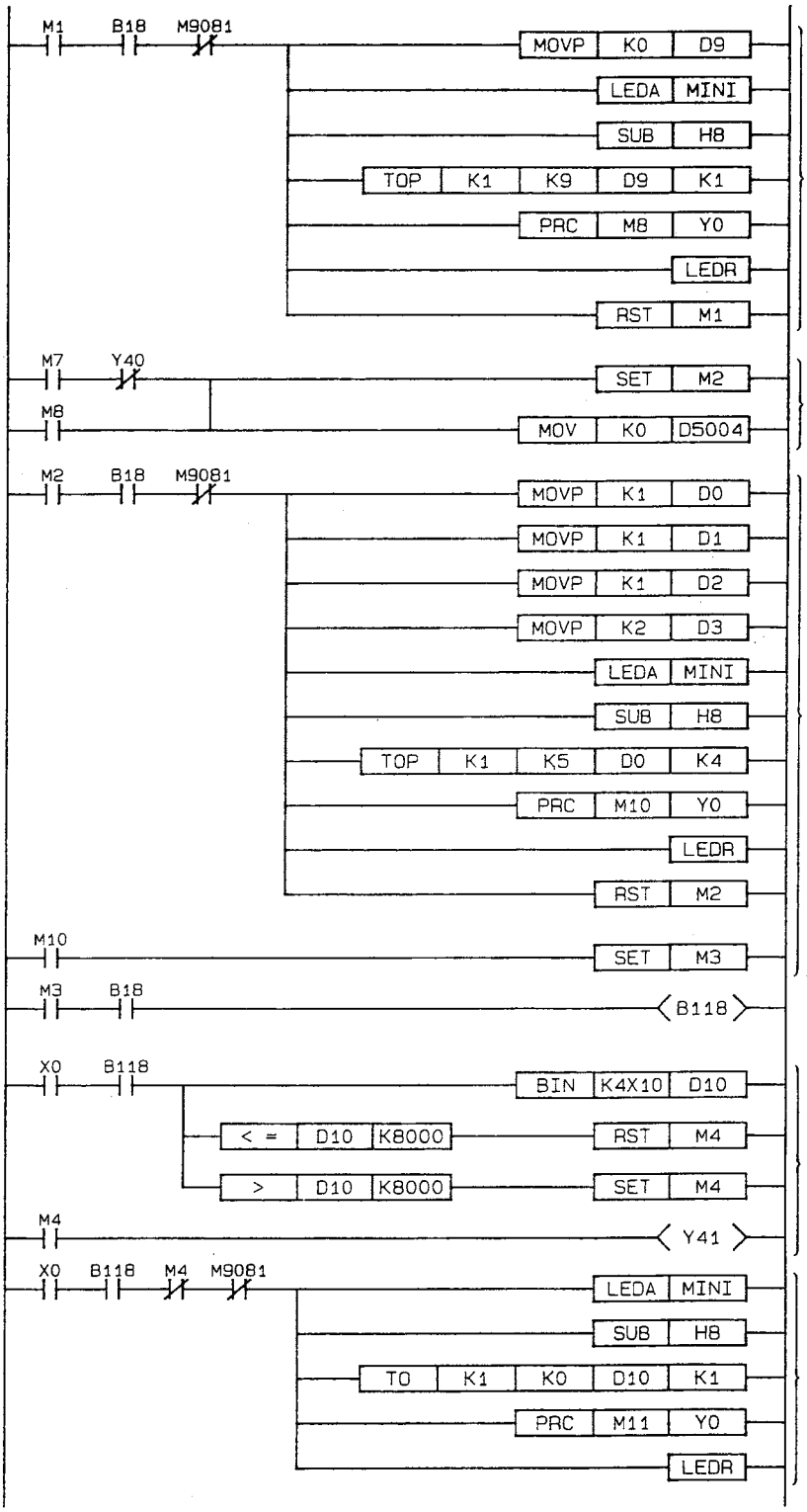
Resets M1-M4 when A64DAVC/DAIC hardware reset operation, communication error or communication response monitoring time-out occurs.

Sets A64DAVC/DAIC's error reset command (M1) under the following conditions:

(1) Communication error reset command (X1)

(2) CPU reset or A64DAVC/DAIC reset operation

Provides external display (Y40) of No. 1 remote terminal unit error.



Writes 0 to buffer memory address 9 to clear error code of A64DAVC/DAIC when A64DAVC/DAIC's error reset command (M1) is given.

Sets A64DAVC/DAIC's initial setting write command (M2) under the following conditions:
(1) Receive data clear completion signal for No. 1 remote terminal
(2) A64DAVC/DAIC's error code clear signal

(1) Stores A64DAVC/DAIC's initial setting data into D0 to D3 when initial setting write command is given.
D0 to D2: Disable CH2-4 for analog output.
D3: Sets digital value resolution to 1/8000.
(2) Writes D0 to D3 data to A64DAVC/DAIC's buffer memory addresses 5-8 and sets M3.

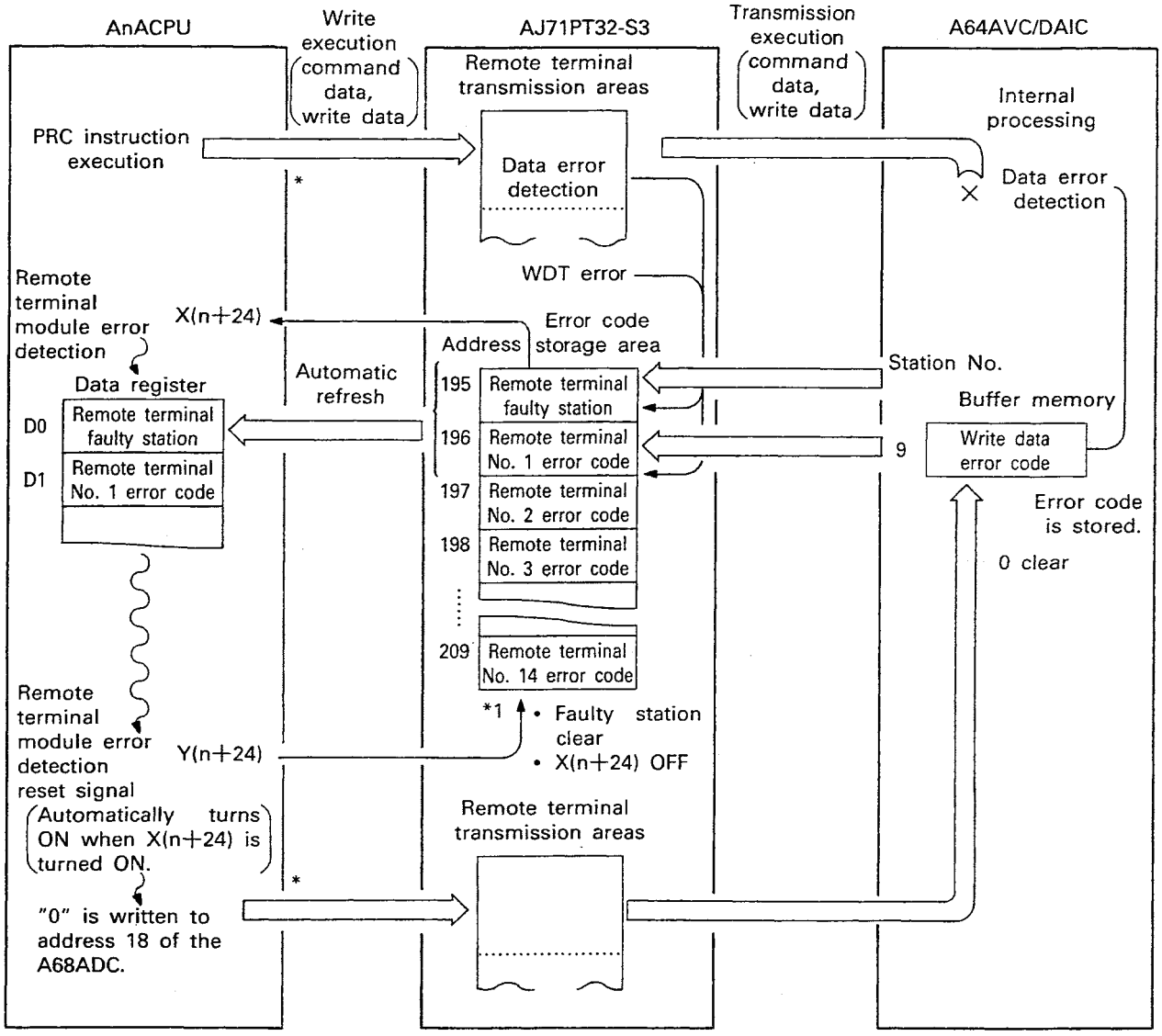
Switches on CH1's analog output enable signal when A64DAVC/DAIC's initial setting write is complete and D/A conversion is ready.

Converts inputs (X20 to X2F) from BCD digital switch into binary and stores results into D10 when digital value setting command (X0) is switched on.
Checks setting range of data stored in D10, and if data is outside setting range, switches on M4 and provides external display (Y41).

Writes D10 data to A64DAVC/DAIC buffer memory address 0 if D10 data is within setting range when digital value setting command (X0) is switched on.

4.7 Error Detection

The figure below shows the detecting procedure when errors have occurred when the AnACPU, A64DAVC/DAIC and AJ71PT32-S3 are used together.



Processings marked * by an asterisk are executed by the sequence program.

- When the remote terminal module error detection signal $X_{(n+24)}$ is turned ON, the AnACPU clears the FROM/TO instruction information for the corresponding remote terminal stored in the communication request registration areas, turns OFF the transmission request signal $Y_{(n+0)}$, and then, turns ON the remote terminal module error detection reset signal $Y_{(n+24)}$ for 1 scan.

5. LINKING TO THE ACPU AND THE AJ71PT32-S3

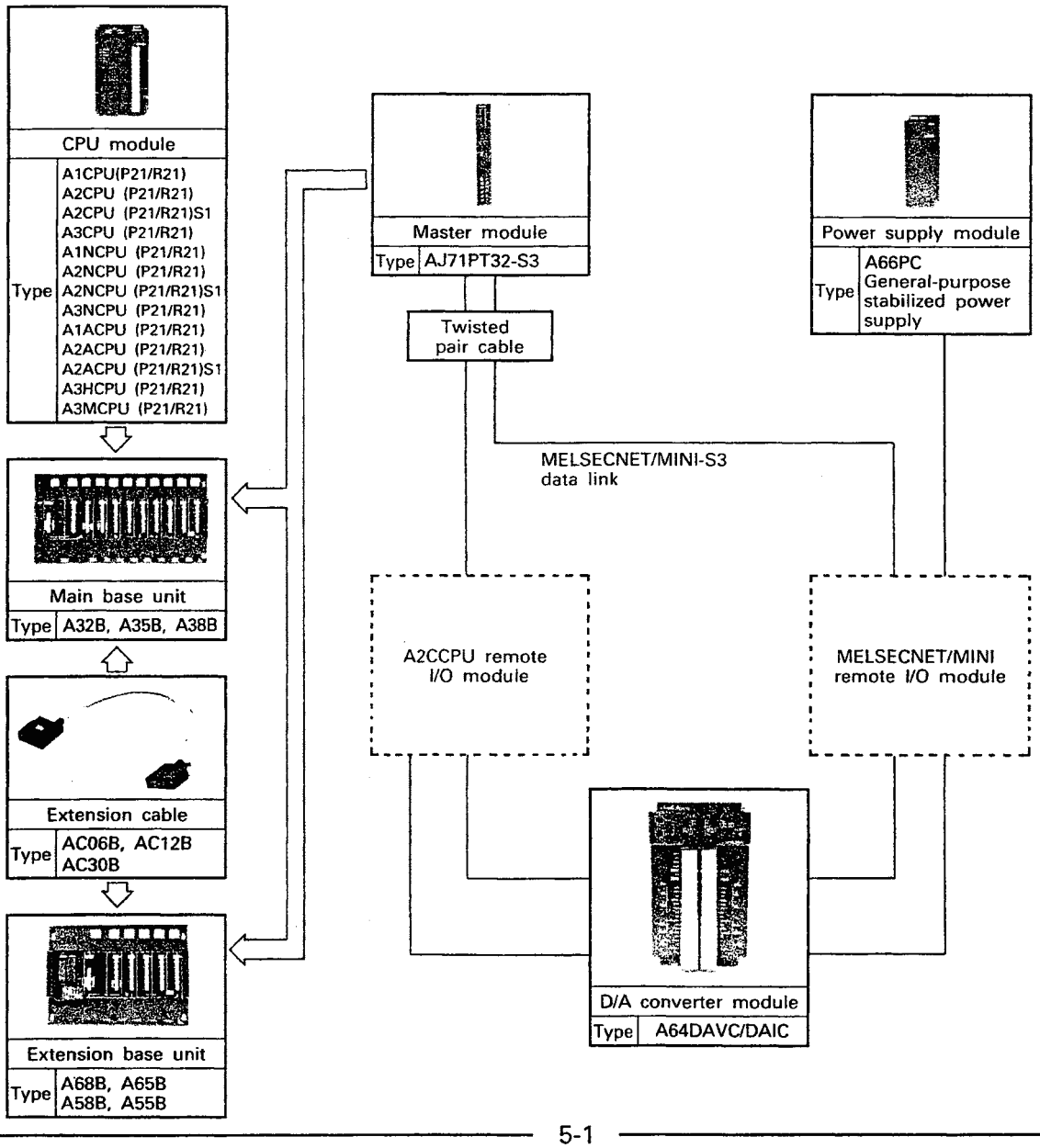
This section gives the linking procedures when an ACPU and AJ71PT32-S3 are used together and linked with the A64DAVC/DAIC on the MINI-S3 link.
The linking procedures when the MINI-S3 dedicated instructions are not used for the programs for the AnACPU in a system configuration which employs the combination of an AnACPU with the AJ71PT32-S3 are the same as those explained herein.

5.1 System Configuration

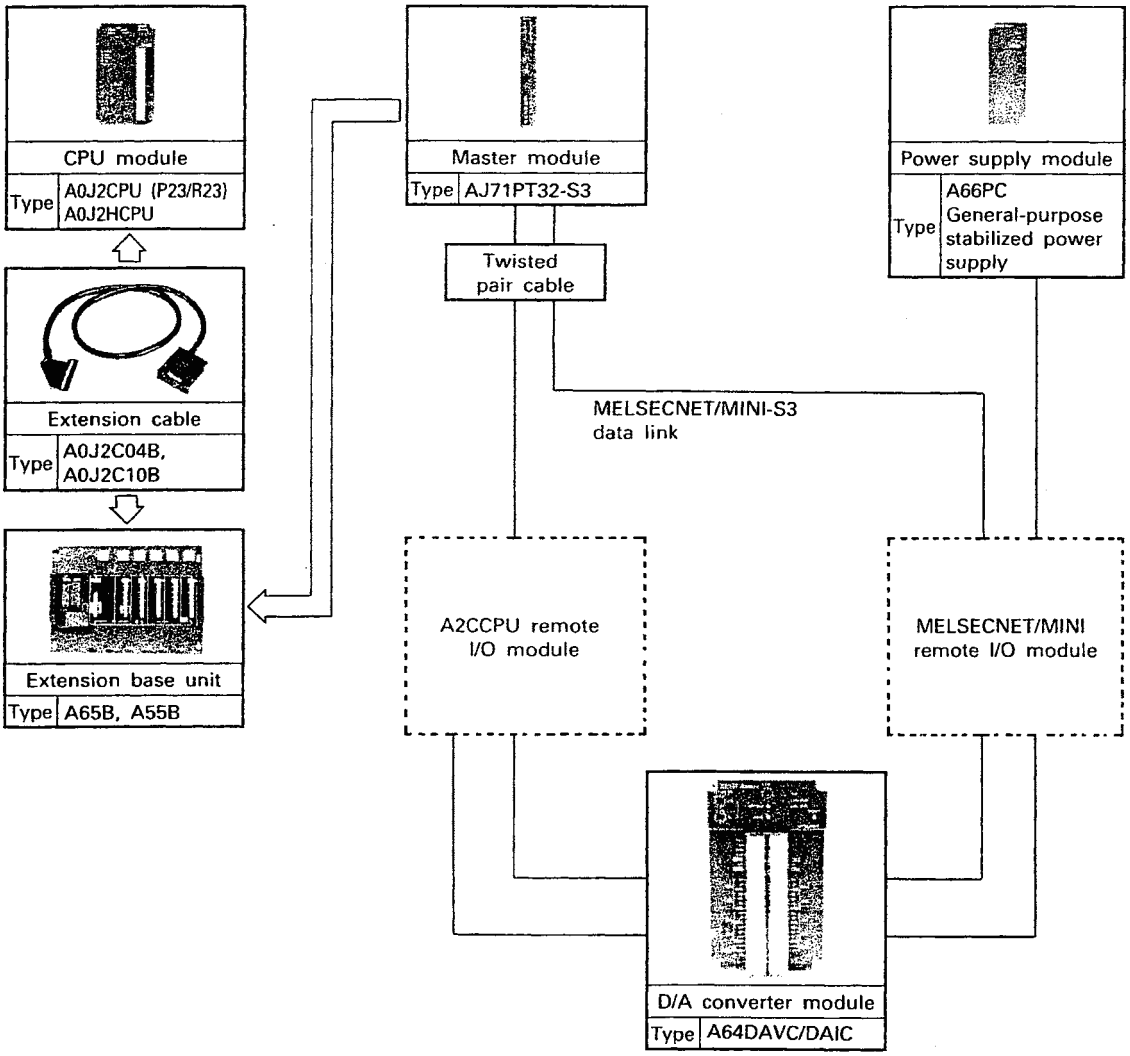
The following diagram shows the system configuration when the A64DAVC/DAIC is used as a remote terminal module of the MELSECNET/MINI-S3 with the AJ71PT32-S3 master module linked to the building block type CPU or the compact type CPU.

5.1.1 Overall configuration

(1) When the building block type CPU is used:



(2) When the compact type CPU is used:



5.1.2 Applicable system modules

The A64DAVC/DAIC can be used as a remote terminal module of the MELSECNET/MINI-S3 link with the AJ71PT32-S3 as its master module.

(1) A maximum of 14 remote terminal modules such as the A64DAVC/DAIC can be connected to an AJ71PT32-S3 module. The following types of modules are used as remote terminal modules.
- A68ADC (analog/digital converter module)
- AD61C (high speed counter module)
- A64DAVC (digital/analog voltage converter module)
- A64DAIC (digital/analog current converter module)
- AJ35PTF-R2 (RS232C interface module)
- AJ35PT-OPB-MI (mounting type operation box)
- AJ35T-OPB-PI (portable type operation box)

(2) Remote modules connected to the AJ71PT32-S3 can occupy up to 64 stations.

(3) The AJ71PT32-S3 can be connected to an independent CPU system or to the master station or a local station of the MELSECNET data link system. It cannot be connected to a remote I/O station.
The number of modules connected to one CPU module is not limited.

REMARK

For details of the MELSECNET/MINI-S3 link system, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

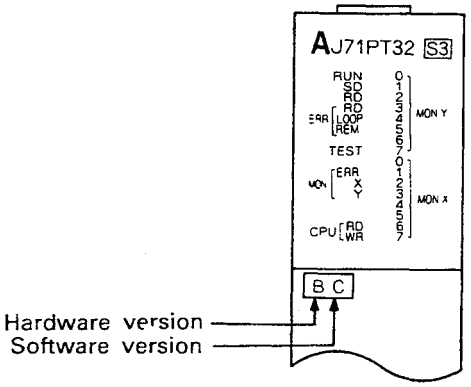
5.1.3 Cautions on constructing the system

(1) Twisted pair cables are used for connection between the AJ71PT32-S3 (master module) and the A64DAVC/DAIC. The maximum connecting distance between stations varies with cable size when twisted pair cables are used.

0.2 mm^2 to smaller than 0.5 mm^2 ····· 50 m
0.5 mm^2 and larger ····· 100 m

(2) The A64DAVC/DAIC requires external supply of 24 VDC power for internal power supply. Use the A66PC power supply module or a general-purpose stabilized power supply (24 VDC). If one power supply is connected to two or more A68ADC or remote I/O modules, select proper cables and wiring route considering voltage drop due to cables. Refer to Section 3.1.2 (3) for calculation of voltage drop.

(3) The AJ71PT32-S3 (master module) of which software version is C or later can be connected to the A64DAVC/DAIC. The modules of which software version is A, B or not specified on the front side cannot be used.



(4) AJ71PT32-S3 cannot be installed to the last slot of 7th extension stage of the A3CPU (P21/R21)

IMPORTANT

Use the AJ71PT32-S3 (master module) in the extension mode (48 occupied points). Be sure to mount the initial data ROM storing the total number of remote stations and remote terminal data (set station numbers of remote terminal modules and corresponding remote terminal numbers) to the master module.

5.2 Data Communication Processings

5.2.1 Communication processes

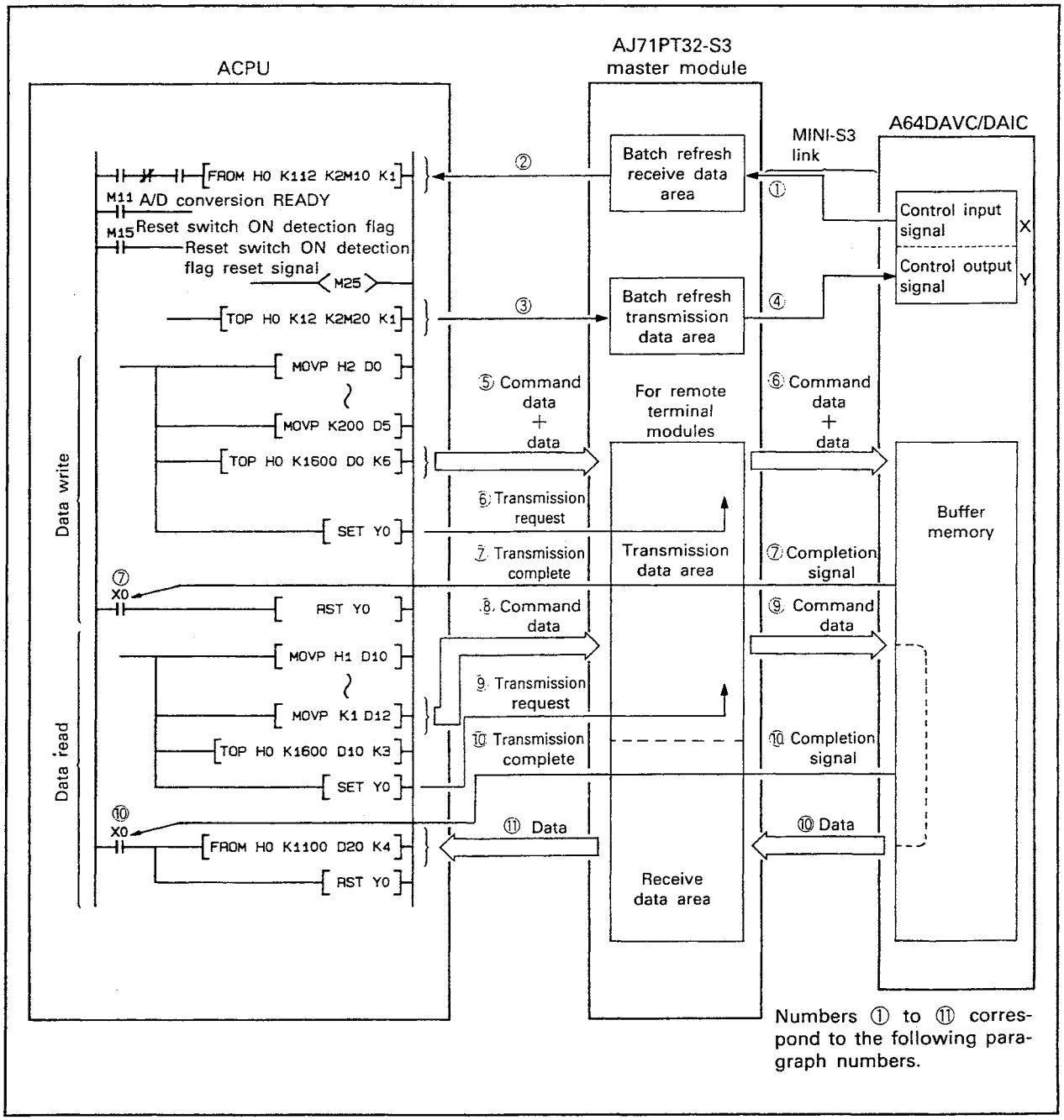


Fig. 5.1 Communication Procedures

(1) Communication processes of control input/output signals used for interlocking of the A64DAVC/DAIC and the ACPU

① Control input signals from the A64DAVC/DAIC are stored automatically in the batch refresh receive data area in the master module at 3.5 to 18 msec intervals.

② Control input signals stored in the batch refresh receive data area are read to designated devices by the FROM instruction.

③ By designating the devices that correspond to the control signals output to the A64DAVC/DAIC with the TO instruction, state data of the designated devices are stored in the batch refresh transmission data area.

④ Control output signals stored in the batch refresh transmission data area are transmitted to the A64DAVC/DAIC at 3.5 to 18 msec intervals.

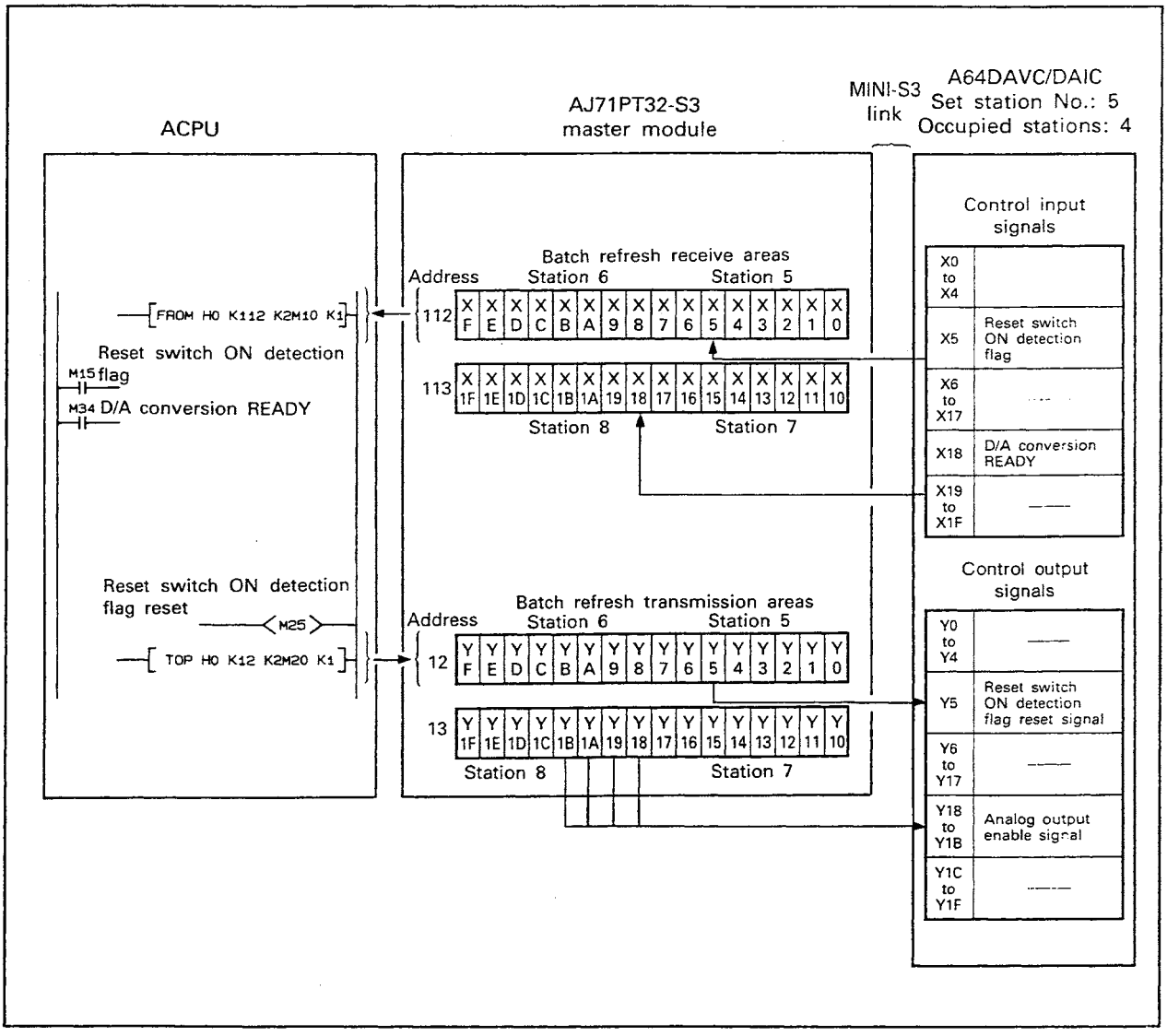


Fig. 5.2 Communication of Control I/O Signals

(2) Writing data to the A64DAVC/DAIC buffer memory

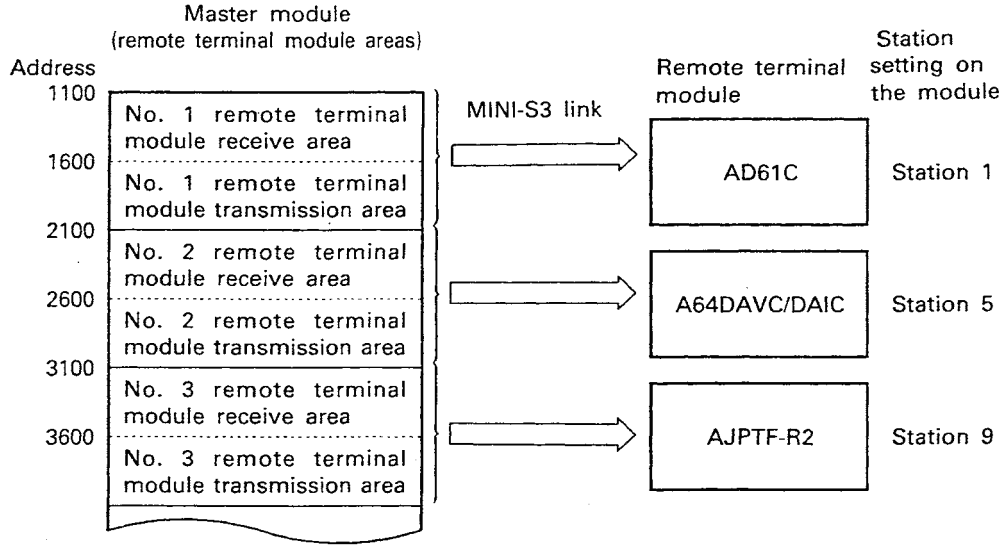
⑤ Command data and write data such as the write execution command to the A64DAVC/DAIC are stored in the remote terminal transmission data area by the TO instruction.

⑥ By execution of the SET $Y_{(n+0)}$ instruction, command data and write data stored in the remote terminal transmission data area are transmitted to the A68ADC.
Transmission data is sent in several times of communication.
The remote terminal module areas correspond to the remote terminal modules connected to the MINI-S3 link as shown below.

When the initial data stored in the initial data ROM mounted to the master module is as shown right:

No. 1 remote terminal = Station 1
No. 2 remote terminal = Station 5
No. 3 remote terminal = Station 9

See Section 4.5.1 for details of the initial data.



⑦ When data is written to the A64DAVC/DAIC buffer memory and internal processing is completed, the completion signal is sent back to the master module.
When the master module has received the completion signal, the transmission completion signal $X_{(n+0)}$ is turned ON.

(3) Reading data from the A64DAVC/DAIC buffer memory

⑧ Command data such as the read execution command from the A64DAVC/DAIC is stored in the remote terminal transmission data area by the TO instruction.

⑨ By execution of the SET $Y_{(n+0)}$ instruction, command data stored in the remote terminal transmission data area is sent to the A64DAVC/DAIC.
Transmission data is sent in several times of communication.

⑩ When the A64DAVC/DAIC has received the command data and after internal processing is completed, the read data is transmitted to the remote terminal receive data area of the master module and the completion signal is sent back.
When the master module has received the completion signal, the transmission completion signal $X_{(n+0)}$ is turned ON.
For details of the transmission completion signal, refer to Section 5.3.2 "Input signals of AJ71PT32-S3".

⑪ After confirming that the transmission completion signal is turned ON, read data stored in the remote terminal receive data area of the master module is read by the FROM instruction.

5.2.2 Processing time

(1) Data write time

Maximum processing time
= 2 scan time + tms × (Number of write data words + 7) + *1 40 ms

(2) Data read time

Maximum processing time
= 2 scan time + 10 ms × (Number of write data words + 8) + *1 40 ms

*1: Internal processing time of the A68ADC

"t" is the I/O refresh time and varies with the number and type of connected remote module stations.
The I/O refresh time is calculated as follows.

Mode	Mode Setting	I/O Refresh Time (ms)
Extension mode (48 points)	Automatic return enable (0)	t = 0.66 + (0.044 × R) + (0.25 × B) + (0.95 × T)
	Automatic return disable (1)	t = 0.54 + (0.058 × R) + (0.25 × B) + (0.95 × T)
	Communication stop at error detection (2)	t = 0.54 + (0.051 × R) + (0.25 × B) + (0.95 × T)

R : Total number of remote stations
B : Number of AJ35PTF-128DT modules
T : Number of remote terminal modules

5.3 I/O Signals Handled With the PLC CPU

5.3.1 I/O signals assigned to the A64DAVC/DAIC

Functions of the control input and output signals handled between the A64DAVC/DAIC and ACPU are described in this section. Devices X refer to the input signals from the A64DAVC/DAIC to the ACPU. Devices Y refer to the output signals from the ACPU to the A64DAVC/DAIC.

Signal Direction: A64DAVC/DAIC → A2CCPU		Signal Direction: A2CCPU → A64DAVC/DAIC	
Device No.	Description	Device No.	Description
X(n+0) to X(n+4)	Unusable	Y(n+0) to Y(n+4)	Unusable
X(n+5)	Reset switch ON detection flag of the A64DAVC/DAIC module	Y(n+5)	Reset switch ON detection flag reset signal
X(n+6) to X(n+17)	Unusable	Y(n+6) to Y(n+17)	Unusable
X(n+18)	D/A conversion READY (1) Turns ON when D/A conversion is ready in the normal mode (other than the test mode) after the A64DAVC/DAIC was turned on or the PLC CPU was reset. (2) Turns OFF when mode is switched from normal to test. (3) Used for the interlock for reading and writing from the PLC CPU to the A64DAVC/DAIC.	Y(n+18)	Analog output enable signal for channel 1 *1
		Y(n+19)	Analog output enable signal for channel 2 *1
		Y(n+1A)	Analog output enable signal for channel 3 *1
		Y(n+1B)	Analog output enable signal for channel 4 *1
X(n+19) to X(n+1F)	Unusable	Y(n+1C) to Y(n+1F)	Unusable

Table 5.1 List of Input/output Signals

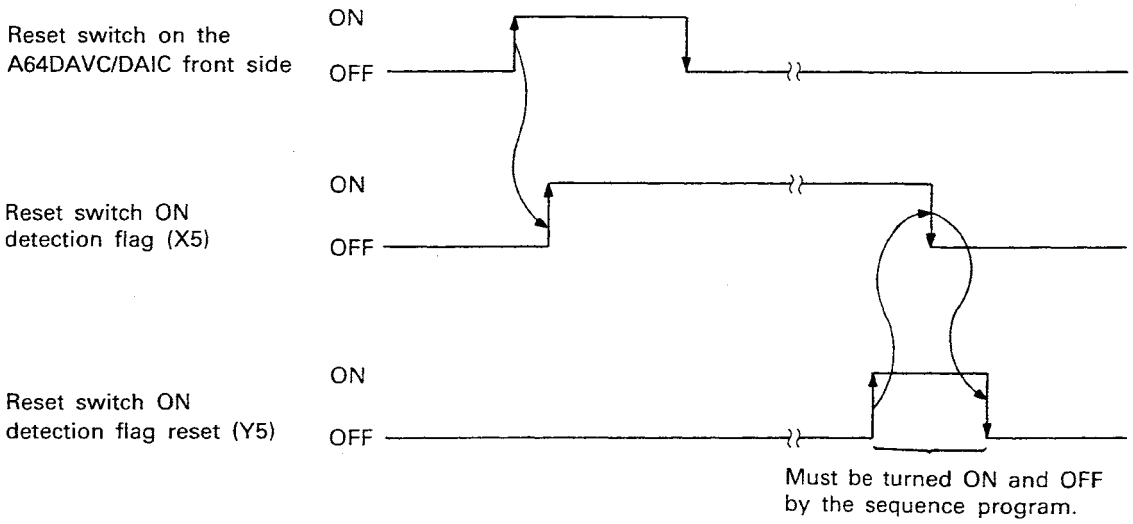
POINT

***1 Analog output enable signals ($Y_{(n+18)}$ to $Y_{(n+1B)}$) change in analog output condition between normal and test modes.**
(1) For analog output in normal mode, see Section 2.2.3 (3).
(2) In test mode, offset/gain values are output without regard to ON/OFF of the analog output enable signal of each channel.

IMPORTANT

Devices $Y_{(n+0)}$ to $Y_{(n+4)}$, $Y_{(n+6)}$ to $Y_{(n+17)}$ and $Y_{(n+1C)}$ to $Y_{(n+1F)}$ are unusable since they are used in the system.
If any of these devices are used (ON/OFF) in the sequence program, functions of the A64DAVC/DAIC are not guaranteed.

(1) Reset switch ON detection flag (X5) and reset switch ON detection flag reset signal (Y5)
Turns ON (latched) when the reset switch of the A64DAVC/DAIC is moved to reset.
To restart communication, turn ON the reset switch ON detection flag reset signal (Y5) with the sequence program.



POINT

(1) If the A64DAVC/DAIC is reset by moving the reset switch, it returns to the initial state. Start operation from the initial setting.
(2) Since X5 turns ON also after the power is turned on, be sure to turn ON Y5 and OFF X5 at the initial stage. And then, execute program for the A64DAVC/DAIC.

5.3.2 I/O signals of the AJ71PT32-S3

Device No.	Signal Name		Device No.	Signal Name	
X (n+0)	Transmission completion signal	For remote terminal module No. 1	Y (n+0)	Transmission request signal	For remote terminal module No. 1
X (n+1)	Read request signal		Y (n+1)	Read completion signal	
X (n+2)	Transmission completion signal	For remote terminal module No. 2	Y (n+2)	Transmission request signal	For remote terminal module No. 2
X (n+3)	Read request signal		Y (n+3)	Read completion signal	
X (n+4)	Transmission completion signal	For remote terminal module No. 3	Y (n+4)	Transmission request signal	For remote terminal module No. 3
X (n+5)	Read request signal		Y (n+5)	Read completion signal	
X (n+6)	Transmission completion signal	For remote terminal module No. 4	Y (n+6)	Transmission request signal	For remote terminal module No. 4
X (n+7)	Read request signal		Y (n+7)	Read completion signal	
X (n+8)	Transmission completion signal	For remote terminal module No. 5	Y (n+8)	Transmission request signal	For remote terminal module No. 5
X (n+9)	Read request signal		Y (n+9)	Read completion signal	
X (n+A)	Transmission completion signal	For remote terminal module No. 6	Y (n+A)	Transmission request signal	For remote terminal module No. 6
X (n+B)	Read request signal		Y (n+B)	Read completion signal	
X (n+C)	Transmission completion signal	For remote terminal module No. 7	Y (n+C)	Transmission request signal	For remote terminal module No. 7
X (n+D)	Read request signal		Y (n+D)	Read completion signal	
X (n+E)	Transmission completion signal	For remote terminal module No. 8	Y (n+E)	Transmission request signal	For remote terminal module No. 8
X (n+F)	Read request signal		Y (n+F)	Read completion signal	
X (n+10)	Transmission completion signal	For remote terminal module No. 9	Y (n+10)	Transmission request signal	For remote terminal module No. 9
X (n+11)	Read request signal		Y (n+11)	Read completion signal	
X (n+12)	Transmission completion signal	For remote terminal module No. 10	Y (n+12)	Transmission request signal	For remote terminal module No. 10
X (n+13)	Read request signal		Y (n+13)	Read completion signal	
X (n+14)	Transmission completion signal	For remote terminal module No. 11	Y (n+14)	Transmission request signal	For remote terminal module No. 11
X (n+15)	Read request signal		Y (n+15)	Read completion signal	
X (n+16)	Transmission completion signal	For remote terminal module No. 12	Y (n+16)	Transmission request signal	For remote terminal module No. 12
X (n+17)	Read request signal		Y (n+17)	Read completion signal	
X (n+18)	Transmission completion signal	For remote terminal module No. 13	Y (n+18)	Transmission request signal	For remote terminal module No. 13
X (n+19)	Read request signal		Y (n+19)	Read completion signal	
X (n+1A)	Transmission completion signal	For remote terminal module No. 14	Y (n+1A)	Transmission request signal	For remote terminal module No. 14
X (n+1B)	Read request signal		Y (n+1B)	Read completion signal	
X (n+1C)	Unusable		Y (n+1C)	Unusable	
X (n+1D)			Y (n+1D)		
X (n+1E)			Y (n+1E)		
X (n+1F)			Y (n+1F)		
X (n+20)	Hardware error		Y (n+20)		
X (n+21)	MINI-S3 link communicating		Y (n+21)		
X (n+22)	Unusable		Y (n+22)		
X (n+23)	Receive data clear completion		Y (n+23)	Receive data clear request	
X (n+24)	Remote terminal module error detection		Y (n+24)	Remote terminal module error detection reset	
X (n+25)	Test mode		Y (n+25)	Unusable	
X (n+26)	MINI-S3 link error detection		Y (n+26)		
X (n+27)	MINI-S3 link communication error		Y (n+27)		
X (n+28)	ROM error		Y (n+28)	MINI-S3 link communication start	
X (n+29)	Unusable		Y (n+29)	Unusable	
X (n+2A)			Y (n+2A)	FROM/TO instruction response designation	
X (n+2B)			Y (n+2B)	Faulty station data clear designation	
X (n+2C)			Y (n+2C)	Buffer memory channel switching	
X (n+2D)			Y (n+2D)	Error reset	
X (n+2E)			Y (n+2E)	Unusable	
X (n+2F)			Y (n+2F)		

Table 5.2 List of I/O Signals

"n" specifies value of the head I/O address of the AJ71PT32-S3.
Example) When the I/O address of the AJ71PT32-S3 is between X/Y20 and X/Y4F: $X_{(n+0)}$ to $X_{(n+2F)}$ = X20 to X4F
$Y_{(n+0)}$ to $Y_{(n+2F)}$ = Y20 to Y4F

REMARK

For details of functions and purposes of control I/O signals, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

5.4 Assignment of Buffer Memory

Assignment of the A64DAVC/DAIC buffer memory (without battery backup) is shown below.

Address		Default	
0	CH1 Digital value setting area	0	Read/write from the PLC CPU is possible.
1	CH2 Digital value setting area	0	
2	CH3 Digital value setting area	0	
3	CH4 Digital value setting area	0	
4	CH1 Analog output enable/disable setting area	0 (Enable)	
5	CH2 Analog output enable/disable setting area	0 (Enable)	
6	CH3 Analog output enable/disable setting area	0 (Enable)	
7	CH4 Analog output enable/disable setting area	0 (Enable)	
8	Digital resolution setting area	1 (1/4000)	
9	Error code storage area	0	

*All 16-bit data.

5.4.1 Contents and data configuration of the buffer memory

Contents of memory items and data configuration of the buffer memory are as follows.

(1) Digital value setting areas for CH1 to CH4 (Addresses 0 to 3)
  (a) Digital values for D/A conversion are written to these areas from the A2CCPU.
  (b) Setting ranges are as shown below.

Module	Digital Value Resolution Setting	Setting Range	Digital Value for D/A Conversion when Values Outside the Specified Ranges are Set.	
A64DAVC	1/4000	−4096 to 4095	−4097 and below: −4096	4096 and above: 4095
	1/8000	−8192 to 8191	−8193 and below: −8192	8192 and above: 8191
	1/12000	−12288 to 12287	−12289 and below: −12288	12288 and above: 12287
A64DAIC	1/4000	0 to 4095	−1 and below: 0	4096 and above: 4095
	1/8000	0 to 8191	−1 and below: 0	8192 and above: 8191
	1/12000	0 to 12287	−1 and below: 0	12288 and above: 12287

  (c) In the cases below, digital values for all channels for D/A conversion turn to 0.
    1) When the D/A conversion READY (X18) is turned ON after the A64DAVC/DAIC was powered on.
    2) When the D/A conversion READY (X18) is turned ON after the A64DAVC/DAIC module was reset.

(2) Analog output enable/disable setting areas for CH1 to CH4 (Addresses 4 to 7)
  (a) Used to set analog output enable/disable after D/A conversion.
  (b) Analog output enable/disable setting is done by writing 1 or 0 to corresponding setting area.
    • 0: Enable
    • 1: Disable

POINT

If a value other than 1 and 0 is written, analog output is processed according to the set data before writing, and the error code is stored in the error code storage area (address 9).

  (c) In the cases below, all channels are set for analog output enable. (Default)
    1) When the A64DAVC/DAIC is powered on.
    2) When the A64DAVC/DAIC module was reset.

(3) Digital value resolution setting area (Address 8)
  (a) Used to set digital value resolution with respect to analog output voltage range.
    Resolution setting is common to all channels.
  (b) Setting values are 1/4000, 1/8000 and 1/12000.
    Values 1, 2 and 3 are used with 1/4000 resolution as the standard value.

Example) To set resolution at 1/8000.

Write "2" in address 8.

1/8000 = 1/4000 (standard) × 2

1/8000 resolution indicates the absolute value range of analog output voltage (0 to ±10 V).

−10 to 0 V, 0 to 10 V (1/8000) (1/8000) ⇨ −10 to 0 to 10 V (1/16000)

POINT

If a value other than 1, 2 and 3 is written, digital value resolution is processed according to the set data before writing or to default, and the error code is stored in the error code storage area (address 9).

  (c) In the cases below, digital value resolution is set at "1" (1/4000). (Default)
    1) When the A64DAVC/DAIC is powered on.
    2) When the A64DAVC/DAIC module was reset.

(4) Error code storage area (Address 9)

(a) When data is read from the PLC CPU, the A64DAVC/DAIC performs data range check and read/write area access checks once respectively. Any value outside the range is stored as error codes in 16-bit binary.
For details of error codes, see Section 7.1.

(b) When several error codes have occurred, the first error code detected by the A64DAVC/DAIC is stored, and the rest are not stored.

(c) To reset an error code, write 0 from the PLC CPU. If an error code is reset, the write data error code is set to "0" and the RUN LED of the A64DAVC/DAIC changes from flickering to illuminating.

5.4.2 Contents and configuration of the AJ71PT32-S3 buffer memory

The AJ71PT32-S3 is provided with a buffer memory (without battery backup) for data communication with the PLC CPU. Use the FROM/TO instructions to read and write data from to the buffer memory.

(1) Assignment of the buffer memory

Address (decimal)		Content	Read/write by PLC CPU
0	(Unused)	—	Read/write enable
1	Retry count	Sets the number of retries when communication error has occurred.	
	(Unused)	—	
4	Line error check	Checks location of line error.	
	(Unused)	—	
10 to 41	Batch refresh transmission data	Writes data to be output to the batch refresh type remote I/O module.	
	(Unused)	—	—
70 to 77	Remote module card information	Stores type identification of each remote module being connected.	Read only
	(Unused)	—	—
90 to 93	Accumulated faulty station detection	Stores faulty remote station numbers. (Detected state is retained until reset.)	Read/write enable
	(Unused)	—	—
100 to 103	Faulty station detection	Stores faulty remote station numbers. (Update state is retained.)	Read only
	(Unused)	—	
107	Communication error code	Stores the cause of the MINI-S3 link communication error signal ON.	
108	Error detection code	Stores accumulated count of the MINI-S3 link error detection ON.	
	(Unused)	—	
110 to 141	Batch refresh receive data	Stores the input data from the batch refresh type remote I/O modules.	
	(Unused)	—	
160	Line error retry counter	Stores the number of retries when communication with all remote modules fails due to line error.	
161 to 192	Retry counter	Stores the number of retries executed to faulty stations.	
	(Unused)	—	
195	Remote terminal module faulty station	Stores the station number when a remote terminal module has caused an error.	
196 to 209	Remote terminal module error code	Stores the cause of the remote terminal module error detection signal X(n+24) ON.	
	(Unused)	—	—
250 to 282	Partial refresh station set data	Writes the station number and digit designation (number of time of division) of the partial refresh type remote I/O module.	Read/write enable
	(Unused)	—	
300 to 363	Partial refresh transmission data	Writes data to be output to the partial refresh type remote I/O module.	
	(Unused)	—	
598	Partial refresh accumulated input error detection	Stores the input faulty station number of the partial refresh type remote I/O module input data. (Detected state is retained until reset.)	
599	Partial refresh input error detection	Stores the input faulty station number of the partial refresh type remote I/O module input data. (Update state of communication is stored.)	
600 to 663	Partial refresh receive data	Stores input data of the partial refresh type remote I/O module.	Read only

Address (decimal)			Content	Read/write by PLC CPU
858	Receive data clear designation		Sets the AJ35PTF-R2 station that clears receive data by the receive data clear request signal Y(n+23).	Read/write enable
859	Receive data clear range designation		Designates the receive buffer that clears receive data by the receive data clear request signal Y(n+23).	
860 to 929	No-protocol mode parameter		Sets the parameters when the AJ35PTF-R2 is used in the no-protocol mode.	
930 to 1099	(Unused)		—	—
	(*1) Channel 0	(*1) Channel 1		
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8	Areas to which transmission data to remote terminal modules is written or to store data received from remote terminal modules. (*1)	Read/write enable
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9		
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10		
4100 to 5099	Communication area for remote terminal No. 4	Communication area for remote terminal No. 11		
5100 to 6099	Communication area for remote terminal No. 5	Communication area for remote terminal No. 12		
6100 to 7099	Communication area for remote terminal No. 6	Communication area for remote terminal No. 13		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14		
	[$Y_{(n+2C)}$: OFF]	[$Y_{(n+2C)}$: ON]		

POINT

(1) Channels specified with *1 are used for executing read/write at areas of addresses 1100 to 8099 and switched by use of the channel switching signal ($Y_{(n+2C)}$).

(2) The buffer memory is all cleard (0 is stored.) at power on or when the PLC CPU is reset. However, retry count (adress 1) and no-protocol mode parameters (adresses 860 to 929) are set at defaults.

(3) Do not write data from the PLC CPU to read only areas.

(4) Unused areas are used by the system of the master module.

(5) Data in the buffer memory can be read continuously including unused areas. For example, data of accumulated faulty stations detection (addresses 90 to 93) and faulty station detection (addresses 100 to 103) can be read by a single FROM instruction.

REMARK

For details of contents at each address and data configuration of the buffer memory, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

(2) Remote terminal communication areas (addresses 1100 to 8099)

(a) Areas for data communication with remote terminal modules.

(b) The communication areas are assigned to two channels. Channel 0 is assigned to remote terminal modules No. 1 to No. 7, and channel 1 is assigned to remote terminal modules No. 8 to No. 14.
Channels are automatically switched according to the remote terminal module station number as designated by the channel switching signal ($Y_{(n+2C)}$).

	Channel 0	Channel 1
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10
4100 7099		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14

The remote terminal module number refers to the number assigned to each remote terminal module set in the initial data ROM of the master module.
Data read/write is executed for areas which correspond to the module numbers assigned to each remote terminal module.

(c) Each communication area consists of a transmission area and a receive area. Capacity of each area at power on is 500 words.

Communication area for remote terminal module No. 1

1100 1599	Receive area (FROM area)
1600 2099	Transmission area (TO area)

The transmission area sets data to be transmitted to remote terminal modules.
The receive area stores data received from remote terminal modules.

(d) Capacity of the transmission and receive areas can be changed by the initial data setting of the master module. (Note that the total capacity of the two areas must not exceed 1000 words.)
Example) Receive area: 200 words, Transmission area: 800 words

5.5 Contents of Initial Setting

The contents of initial setting when the A64DAVC/DAIC is used as a remote terminal module are described.

5.5.1 Initial setting of the AJ71PT32-S3

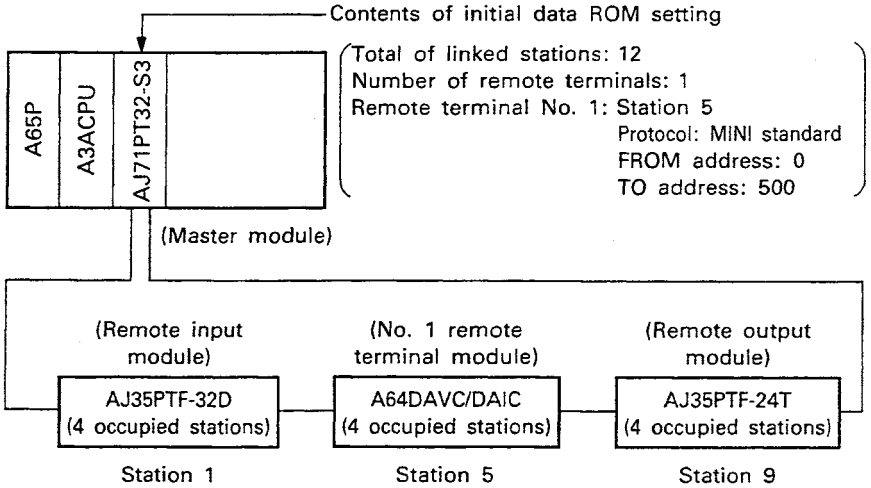
Use the SW□GP-MINIP system disk to set initial data and to store it in the initial data ROM.
The initial data ROM is inserted to the ROM socket of the AJ71PT32-S3.
Contents of initial data setting are mentioned below.

- Total number of remote stations: Set the total number of occupied stations of each module connected to the MINI-S3 link.
  Example) AJ35PTF-32A (remote I/O module) 4 stations
  A64DAVC/DAIC (remote terminal module) 4 stations
  AJ35PTF-24T (remote I/O module) 4 stations
  Total: 12 stations
- Station number of each remote terminal number: Set the station numbers set for modules which correspond to remote terminal modules No. 1 to No. 14.
  Example) AJ35PTF-32A 1 stations
  A64DAVC/DAIC 5 stations ← Remote terminal module
  AJ35PTF-24T 9 stations
  Remote terminal No. 1=5 stations
- Protocol: Set the protocol used for communications with the A64DAVC/DAIC.
  Use the MINI standard protocol.
- Remote terminal FROM/TO area setting:
  Set the capacity for the FROM area and the TO area as explained in Section 5.4.2 (2).
  Default is 500 words for each of the FROM area and the TO area.

For details of setting procedures, refer to SW□GP-MINIP Operating Manual.

5.6 Programming

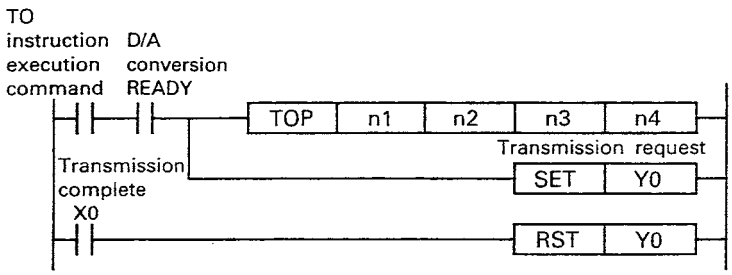
This section describes the programming procedures for writing setting data to the A64DAVC/DAIC and reading digital output values with a system configuration shown below.



5.6.1 Writing data to the A64DAVC/DAIC

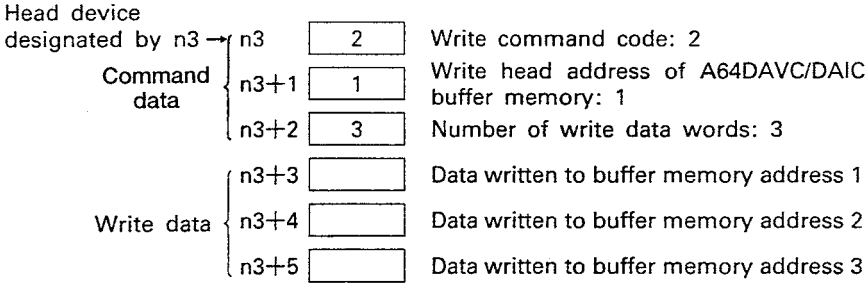
The TO instruction in the sequence program is used to write data to the buffer memory of designated remote terminal module. Items of the buffer memory and procedures of writing to the A64DAVC/DAIC are described below.

(a) Digital value for each channel
(b) Analog output enable/disable setting for each channel
(c) Digital value resolution setting
(d) Error code clear ("0" is written from the ACPU at error code reset.)



n1	Head I/O number assigned to AJ71PT32-S3
n2	Head address of the remote terminal transmission areas
n3	Head device number of data register which stores command data.
n4	Total number of words of command data and write data

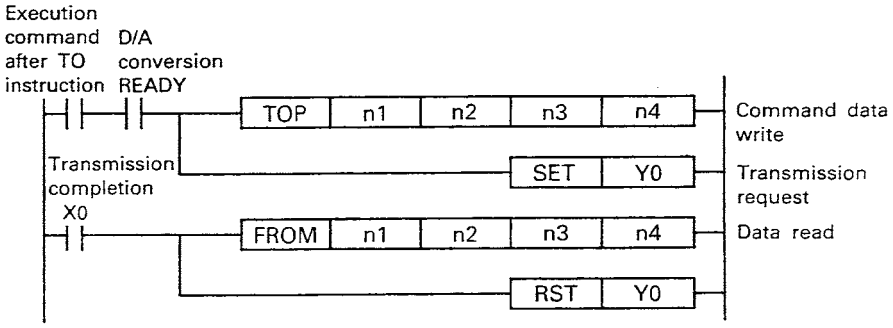
Command data and write data are set as follows.



5.6.2 Reading data from the A64DAVC/DAIC

The FROM instruction is used to read data, which was transmitted from the buffer memory of designated remote terminal module, from the remote terminal receive areas of the master module using the TO instruction in the sequence program.
Items of the buffer memory and procedures of reading from the A64DAVC/DAIC are described below.

(a) Write data error code



Command data write format (TO instruction)

n1	Head I/O number assigned to AJ71PT32-S3
n2	Head address of the remote terminal transmission areas of corresponding remote terminal number assigned by initial data.
n3	Head device number of data register which stores command data.
n4	Total number of words of command data

Command data is set as follows.

Head device designated by n3 → n3	1	Read command code: 1
n3+1	9	Read head address of A64DAVC/DAIC buffer memory: 9
n3+2	3	Number of read data words: 1

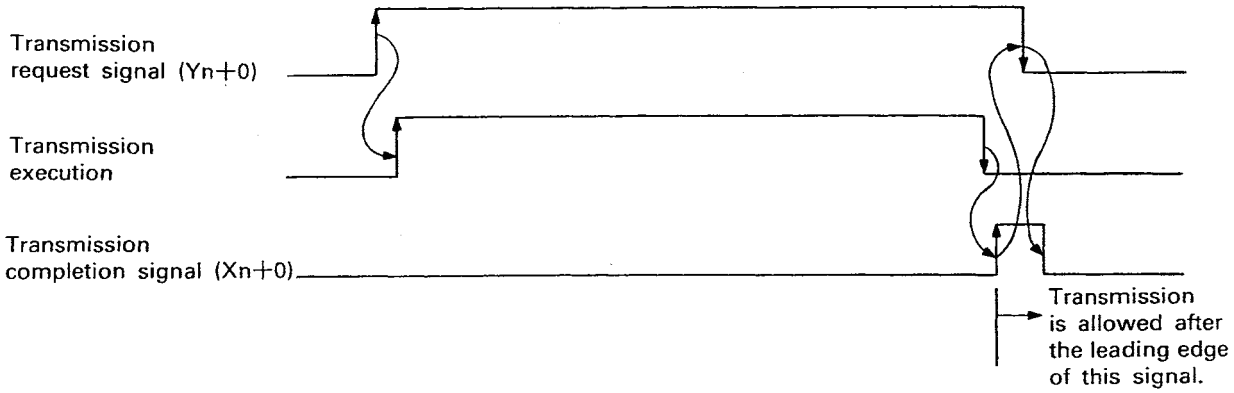
Data read format (FROM instruction)

n1	Head I/O number assigned to AJ71PT32-S3
n2	(Head+1) address of the remote terminal receive areas of corresponding remote terminal number assigned by initial data.
n3	Head device number of data register which stores receive data.
n4	Total number of words of read data

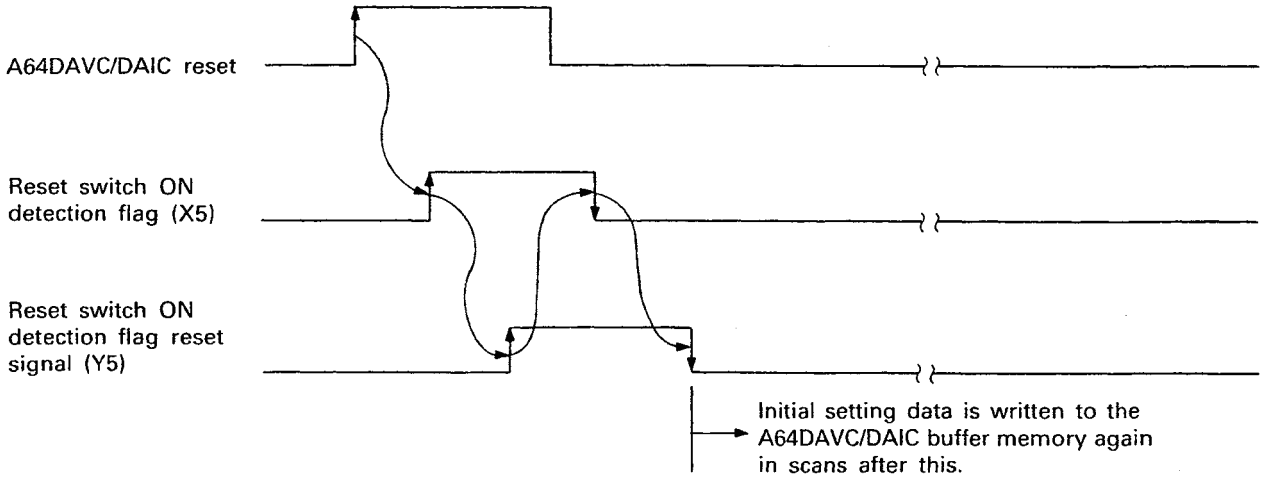
5.6.3 Cautions on programming

(1) For communication with the remote terminal modules linked to the AJ71PT32-S3, turn ON the AJ71PT32-S3 communication start signal $Y_{(n+28)}$ always before execution of each instruction. If the communication start signal has not turned ON, communication processings are not possible.

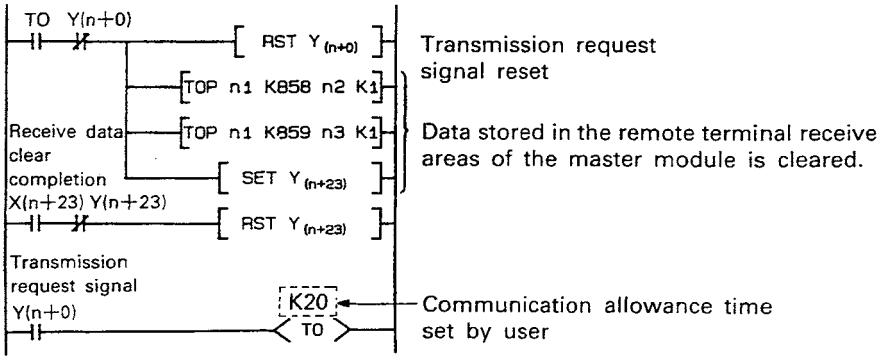
(2) Transmission to a remote terminal module cannot be performed if the transmission request signal previously assigned to the same module remains turned ON. Confirm that the previous transmission is completed with the transmission completion signal, and then, reset the transmission request signal before executing transmission to the same remote terminal module.



(3) When the reset switch on the front of the A64DAVC/DAIC is moved to reset, the A64DAVC/DAIC returns to initial state, and D/A conversion is processed with defaults.
The reset switch ON detection signal from the A64DAVC/DAIC should always be read from the batch refresh receive areas of the master module using the FROM instruction. Initial set data should be transmitted to the A64DAVC/DAIC when the detection signal has turned ON. (when initial set data is other than default)



(4) If a communication completion response signal to the transmission executed to the A64DAVC/DAIC is not sent back, the CPU module is set in the state waiting for the communication completion signal infinitely unless the CPU module is reset. To prevent the infinite completion wait state, provide a monitoring timer to turn off the transmission request signal and to clear data stored in the remote terminal receive areas when the timer has timed out, as shown below.

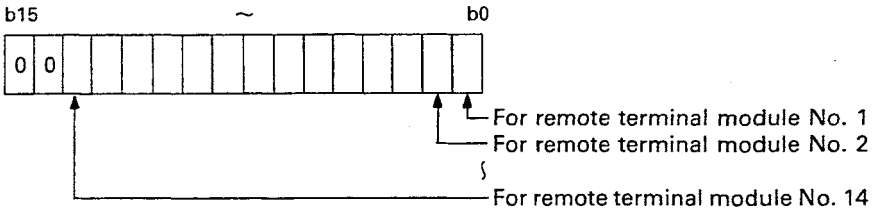


$X_{(n+28)}$, $Y_{(n+0)}$ and $Y_{(n+23)}$ are control I/O signals for the AJ71PT32-S3. See Section 5.3.2 for details.

Contents of n_1, n_2 and n_3 designated by each instruction are as described below.

n_1: Higher 2 digits of head I/O number assigned to AJ71PT32-S3
Example) "12_H" when assigned to X/Y120 to 13F.

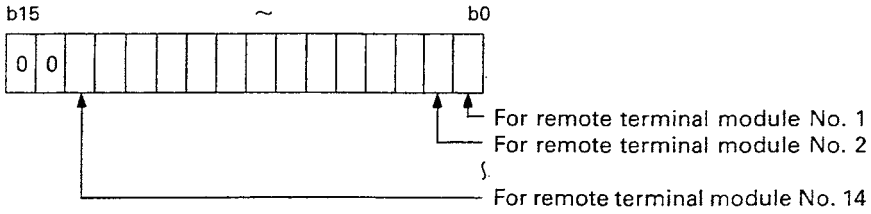
n_2: Receive buffer clear/no clear setting for each remote terminal number



0: No clear
1: Clear

Contents of setting are written to address 858 in the AJ71PT32-S3 buffer memory.

n3: Clear execution range setting for each remote terminal number

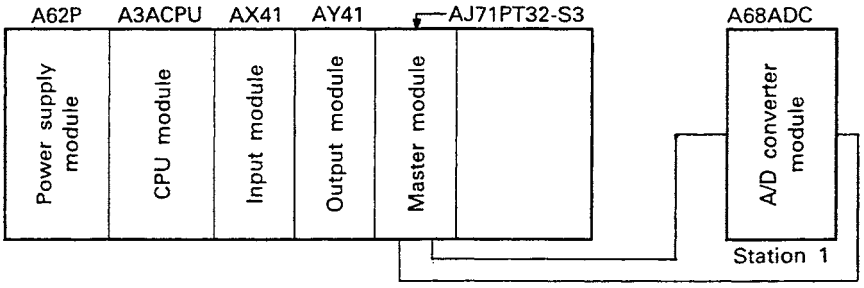


0: Only the remote terminal receive areas of the master module are cleared.
1: The remote terminal receive areas of the master module and the A64DAVC/DAIC receive buffer are cleared.

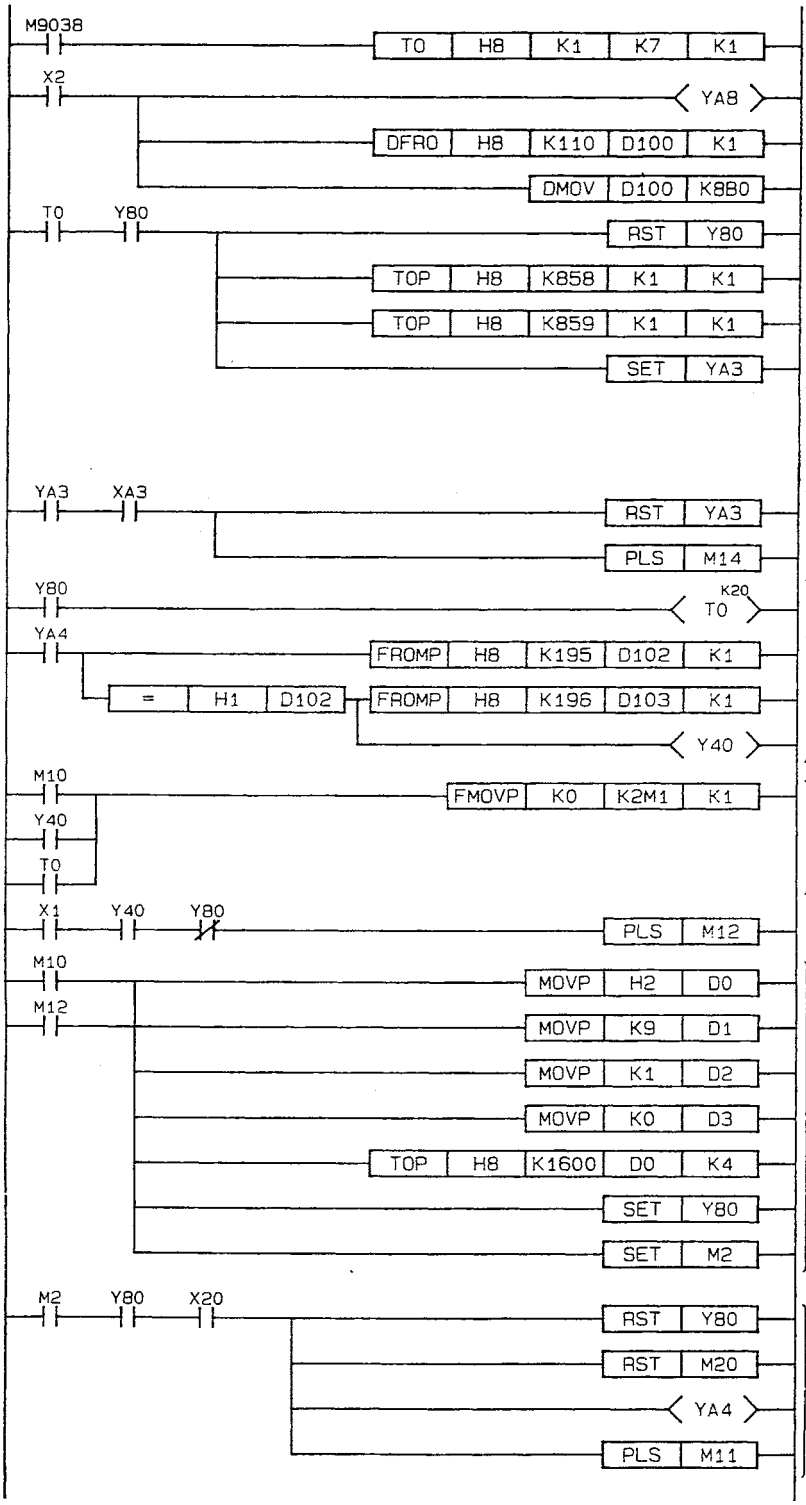
Contents of setting are written to address 859 in the AJ71PT32-S3 buffer memory.

5.6.4 Program example

The program example shown in this section writes the value (0 to 8000) set by the BCD digital switch to channel 1 of the A64DAVC/DAIC in the following system configuration.
The resolution of the digital value is assumed to be 1/8000 and channels 2 to 4 to be disabled for analog output.



1) Master module's initial data ROM settings
   Total number of link stations: 4
   Number of remote terminals: 1
   No. 1 remote terminal: Station 1
   Protocol - MINI-standard
   FROM address - 0
   TO address - 500
2) Program example
   - Switching "on" X2 (MINI-S3 link communication start command) of the input module starts MINI-S3 link.
   - Starting the MINI-S3 link communication enables channel 1 for analog output and switching "on" X0 (digital value setting command) of the input module writes the values of X10 to X1F (digital value setting, BCD 4 digits) to the A64DAVC/DAIC.
   - Any digital value setting greater than 8000 switches "on" Y41 of the output module and is displayed by an external device.
   - Detection of a communication error with the remote terminal unit switches "on" Y40 to stop all processings.
   - Switching "on" X1 (communication error detection flag reset command) clears all the error status area and flags.
   - Resetting the A64DAVC/DAIC stops all processings.
   - Switching "on" B5 (reset "on" detection flag) clears all.



Sets the number of communication retries "seven times" to master module buffer memory address 1.

Starts MINI-S3 link communication when MINI-S3 link communication start request (X2) is switched on and reads continuously reads A64DAVC/DAIC's control station input signal to B0 to B1F.

Performs the following processings when communication response monitoring time-out occurs:

(1) Switches off transmission request signal to No. 1 remote terminal (Y80).

(2) Specifies clearing of master module's receive area for No. 1 remote terminal and sets receive data clear request signal (YA3).

Switches on M14 on receive data clear completion (XA3) and resets receive data clear request.

Communication response monitoring time is set by user.

Provides external display (Y40) of No. 1 remote terminal error and reads error code to D103.

Resets M1 to M4 when A64DAVC/DAIC hardware reset operation, communication error or communication response monitoring time-out occurs.

Communication error reset command

Writes D0 to D3 data to master module's transmission area for No. 1 remote terminal and sets write transmission request signal (Y80).

D0: Write command data.

D1: Head address of A64DAVC/DAIC buffer memory.

D2: Number of words of data to be written

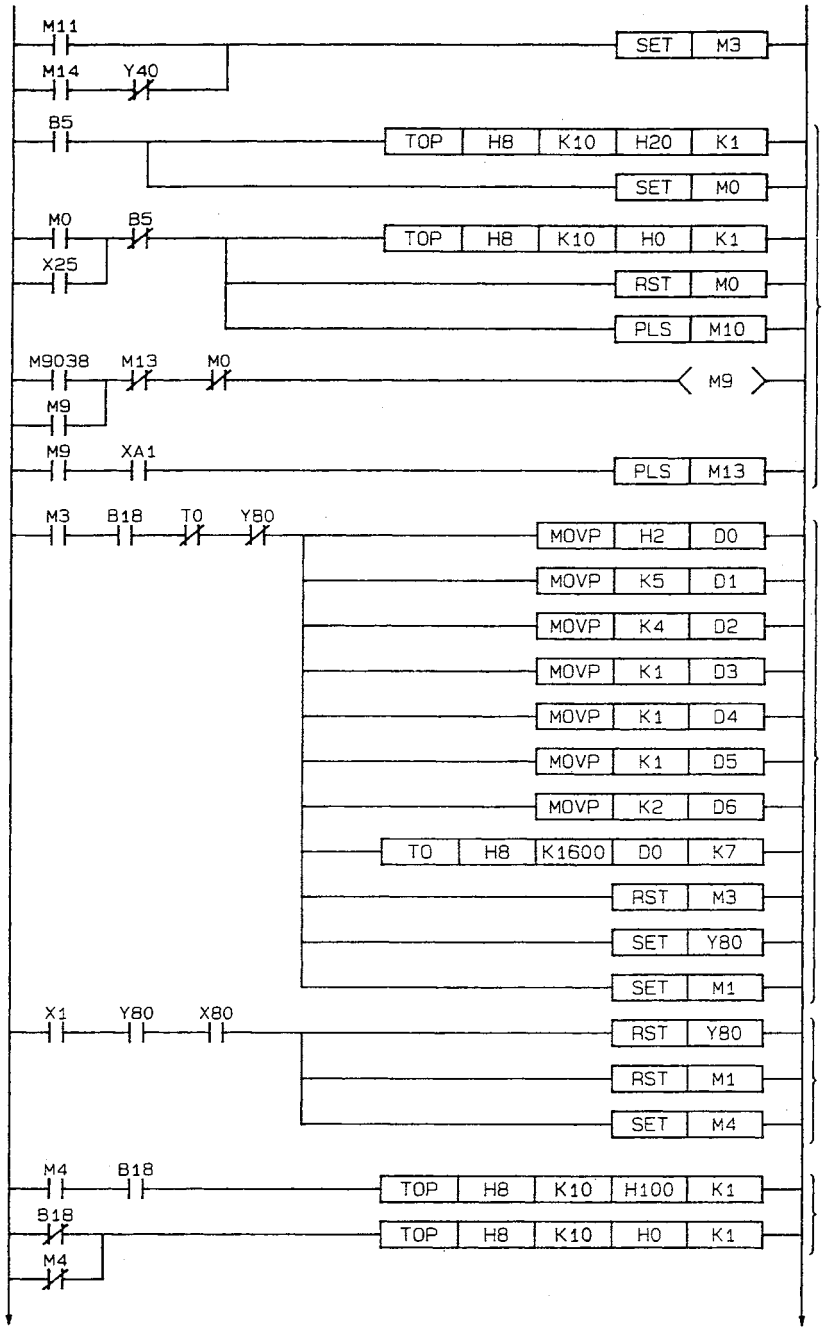
D3: Data to be written

Performs the following processings when transmission to No. 1 remote terminal is complete:

(1) Resets transmission request signal.

(2) Resets remote terminal error detection.

(3) Switches on M11 when communication error reset is complete.



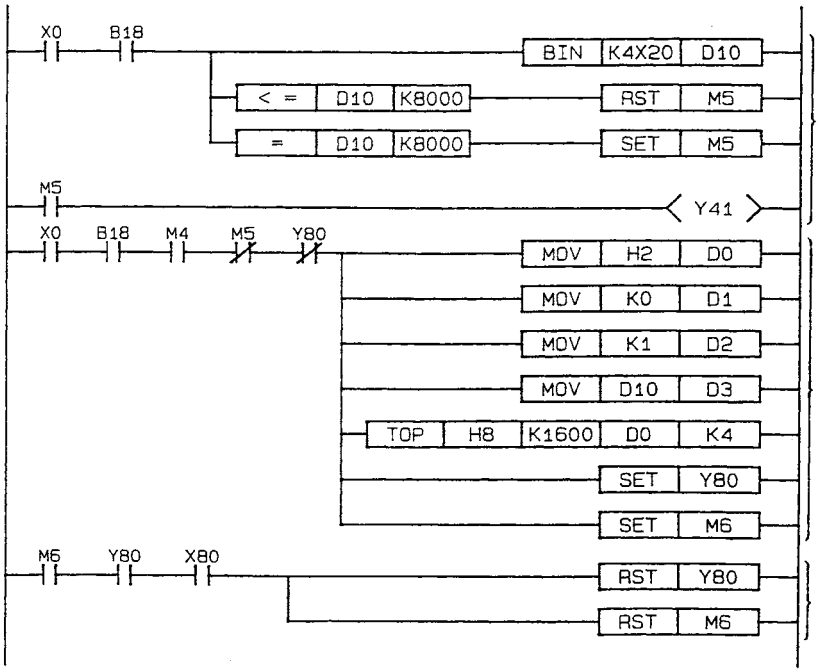
Sets A64DAVC's initial setting write command (M3) when communication error reset is complete or receive data clear is complete.

(1) Resets reset switch ON detection flag when A64DAVC/DAIC hardware reset is performed.
(2) Switches on M10 when above processing is complete or CPU is reset.

Writes D0 to D6 data to master module's transmission area for No. 1 remote terminal and sets transmission request signal (Y80).
D0: Write command code
D1: Head address of A64DAVC/DAIC buffer memory
D2: Number of words of data to be written
D3 to D5: Disable CH2 to 4 for analog output.
D6: Sets digital value resolution to 1/8000.

Resets transmission request signal (Y80) and sets M4 when transmission of data set by M1 is complete.

Switches on CH1's analog output enable signal when A64DAVC/DAIC's initial setting write is complete and D/A conversion is ready.



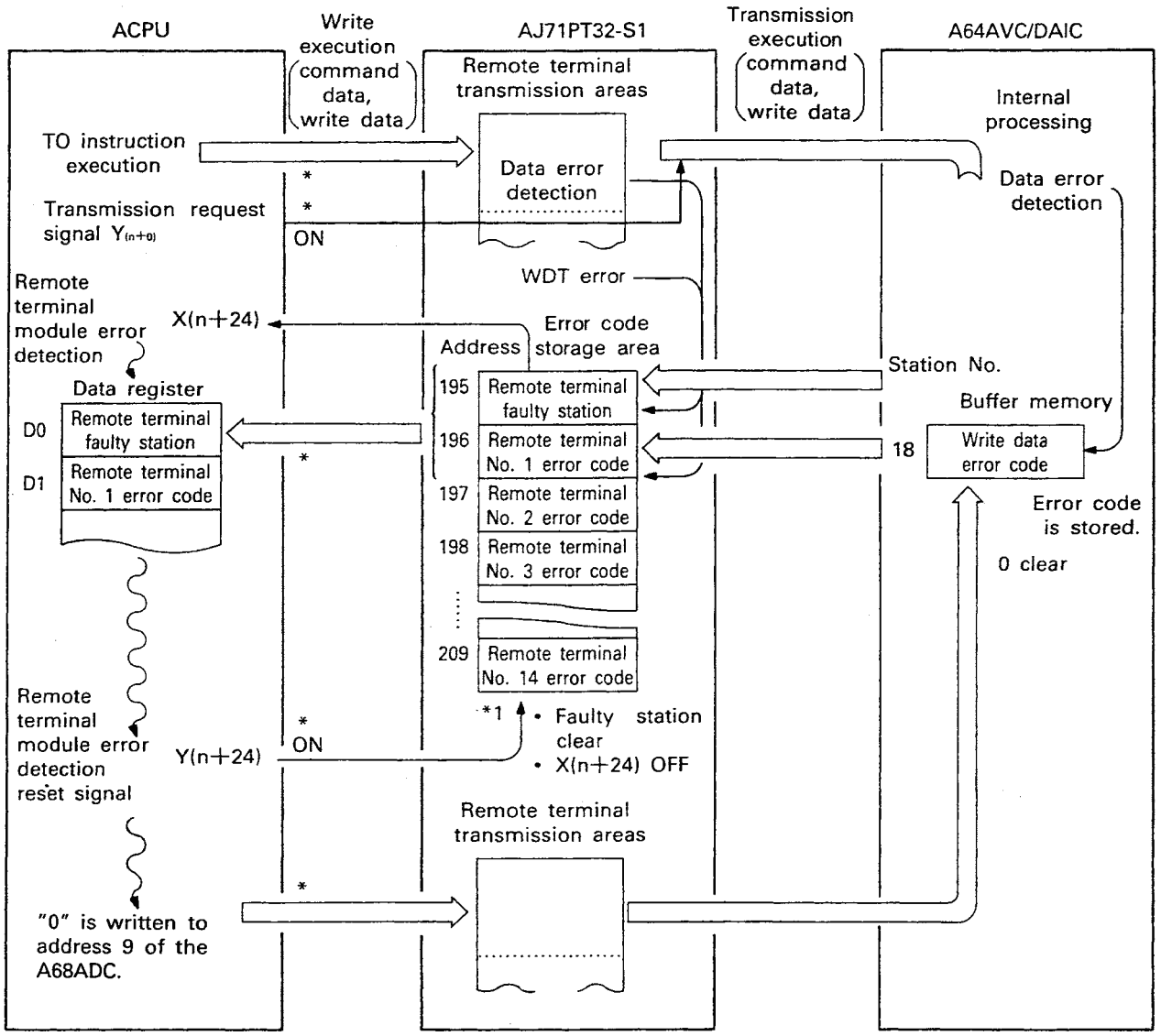
Converts inputs (X20 to X2F) from BCD digital switch into binary and stores results into D10 when digital value setting command (X0) is switched on.
Checks setting range of data stored in D10, and if data is outside setting range, switches on M5 and provides external display (Y41).

Writes D10 data to master module's transmission area for No. 1 remote terminal and sets transmission request signal (Y80) if D10 data is within setting range when digital value setting command (X0) is switched on.
D0: Write command code
D1: Head address of A64DAVC/DAIC buffer memory
D2: Number of words of data to be written
D3: Data to be written

Resets transmission request signal (Y80) when transmission of data set by M6 is complete.

5.7 Error Detection

The figure below shows the detecting procedure when errors have occurred when the AnACPU, A64DAVC/DAIC and AJ71PT32-S3 are used together.



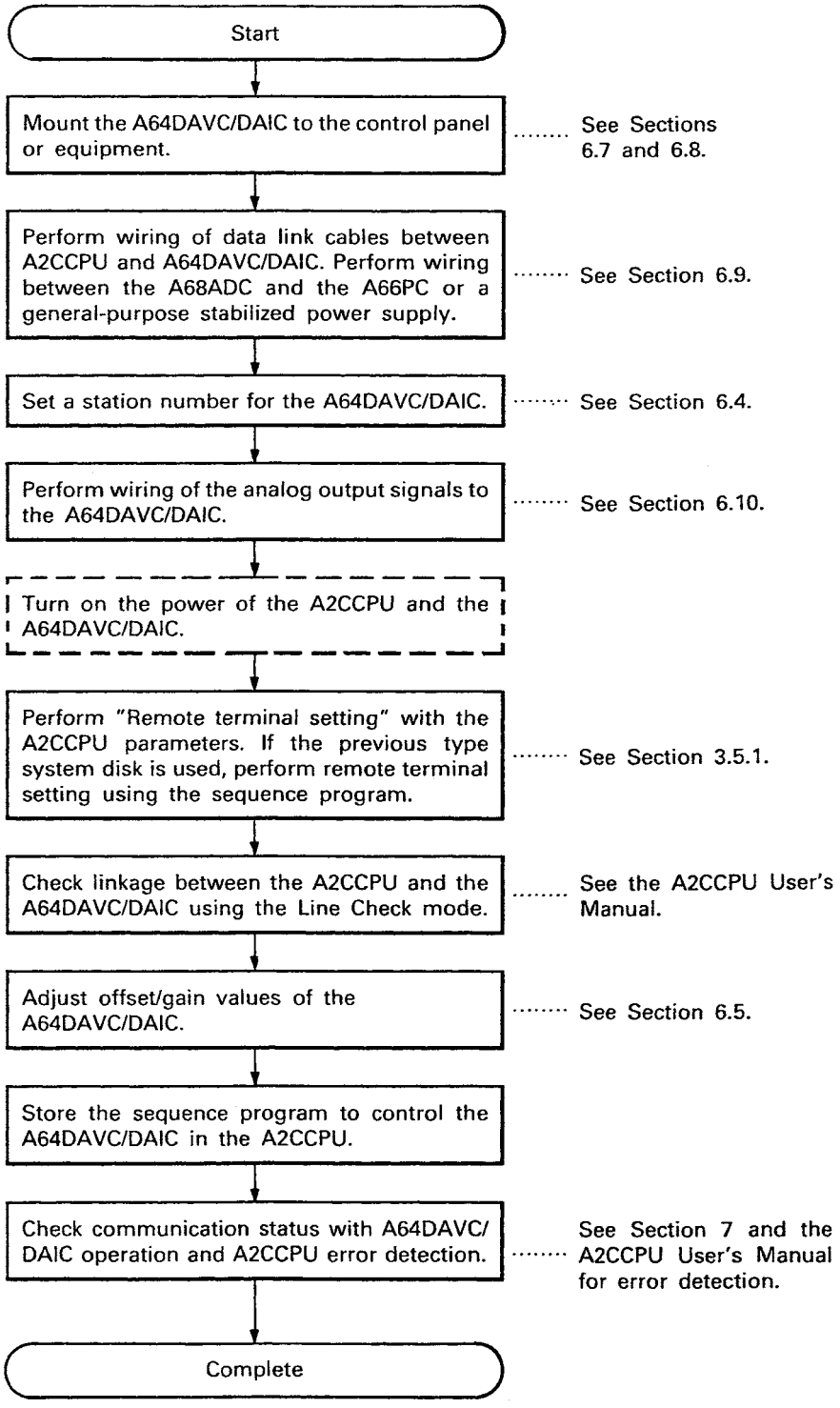
Processings marked * by an asterisk are executed by the sequence program.

6. INSTALLATION AND PRE-OPERATION SETTING PROCEDURES

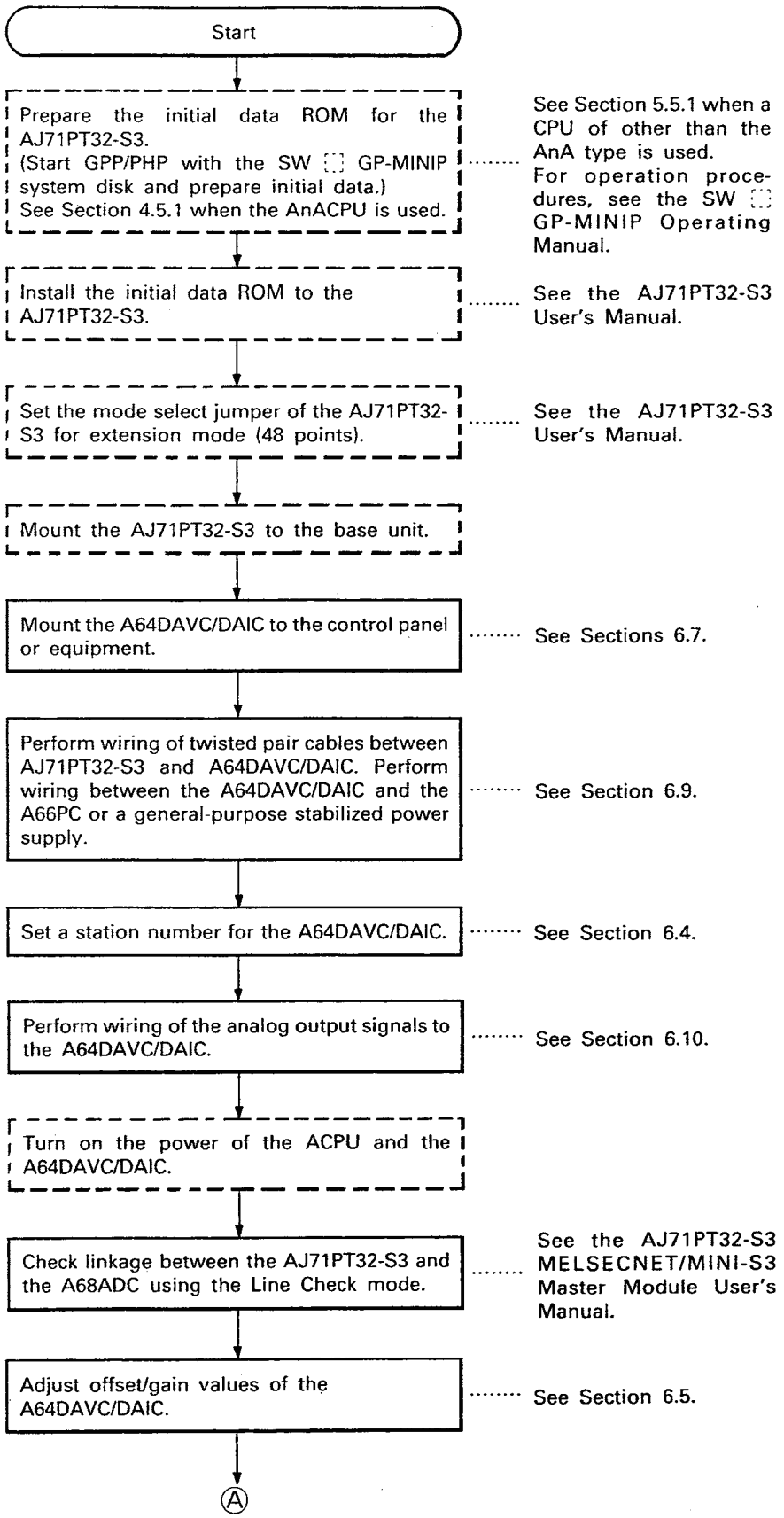
6.1 Pre-operation Setting Procedures

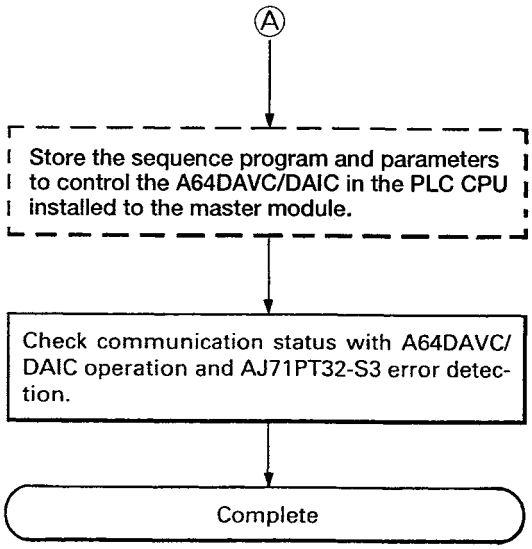
This section gives setting procedures required before starting operation of the A64DAVC/DAIC when used with the A2CCPU and with the AJ71PT32-S3.

(1) When the A2CCPU is used:



(2) When the AJ71PT32-S3 is used:





See Sections 4.5.2 and 4.6 when the AnACPU is used.
See Section 5.6 when a CPU of other than the AnA type is used.

See the AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual for error detection.

6.2 Handling Instructions

(1) Protect the A64DAVC/DAIC and its terminal block from impact.

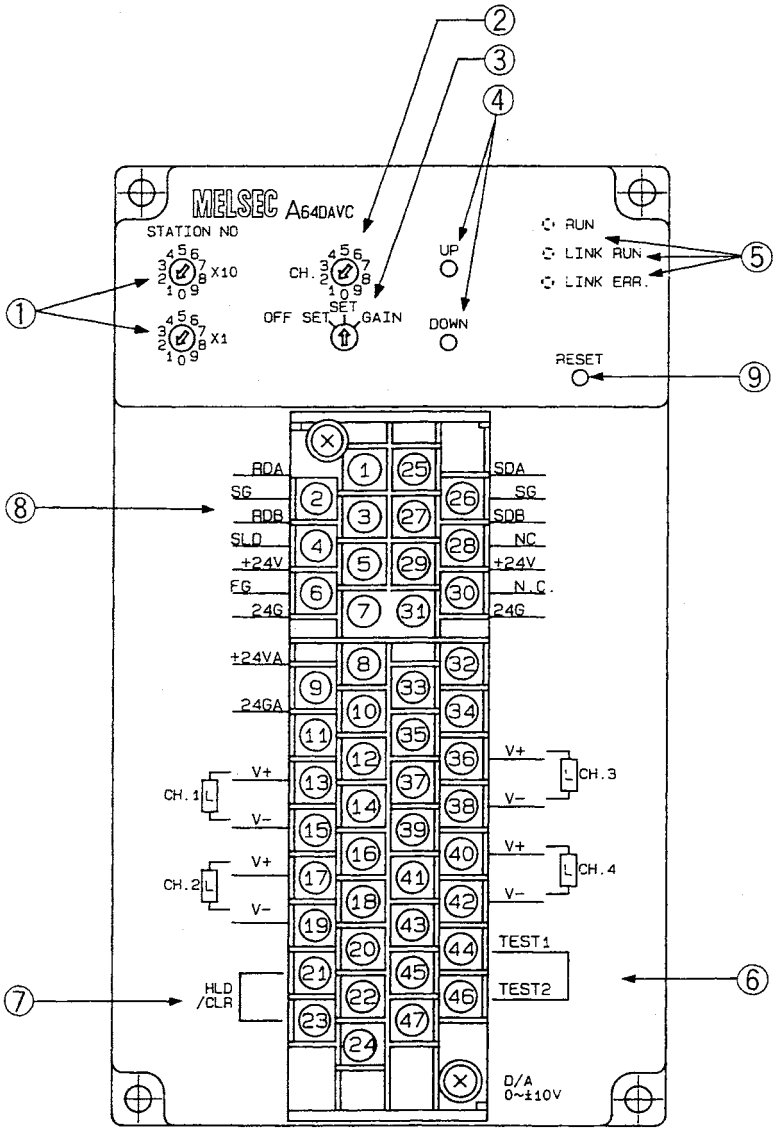
(2) Do not touch or remove the printed circuit board from the case.

(3) When wiring, ensure that no wire offcuts enter the module and remove any that do enter.

(4) Tighten terminal screws as specified below.

Screw	Tightening Torque Range N·cm
I/O terminal block terminal screw (M3.5 screw)	59 to 88
I/O terminal block mounting screw (M4 screw)	78 to 118

6.3 Part Identification



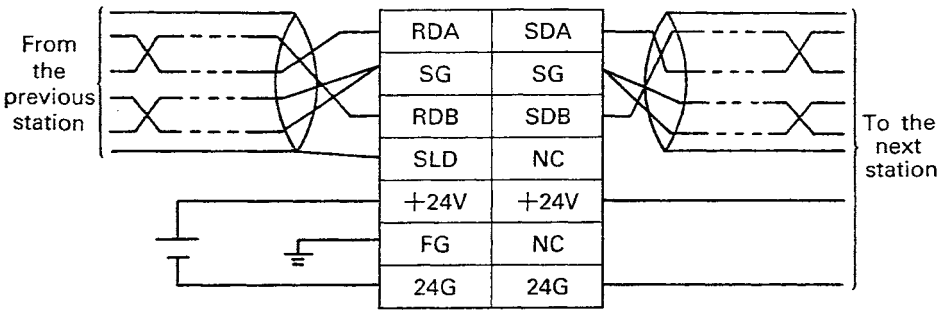
<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>Station number setting switches</td><td>⓪×10
⓪×1
Used to set the station number of the A64DAVC/DAIC in a range from 1 to (64 − occupied stations + 1).
See Section 6.4.</td></tr>
<tr><td>2</td><td>Channel select switch</td><td>Used to select the channel for offset/gain adjustment.
(Positions 0 and 5 to 9 select no processing.)</td></tr>
<tr><td>3</td><td>OFFSET/GAIN setting switch</td><td>Used to set offset/gain values in test mode.
(1) OFFSET: Offset value calibration
(2) GAIN: Gain value calibration
(3) SET: Offset/gain value storage
(Analog output when this switch is turned from OFFSET/GAIN to SET is stored as offset/gain value in the internal memory of the A64DAVC/DAIC.)</td></tr>
<tr><td>4</td><td>UP/DOWN switches</td><td>Used to adjust analog output of offset/gain of specified channel. Turning ON the UP/DOWN switches makes analog output increase/decrease.</td></tr>
<tr><td>5</td><td>Operation state indicator LEDs</td><td>
<table>
<tr><td rowspan="2">RUN</td><td>Normal mode</td><td>On: Normally running
Flicker: Read/write data error
Off: 24 VDC is off or WDT error.</td></tr>
<tr><td>Test mode</td><td>Flicker: Flickers at 0.5 sec intervals when the OFFSET/GAIN switch is in the OFFSET or GAIN position.
Flickers at 0.1 sec intervals when analog output exceeded the upper or lower limit of the setting range when the UP/DOWN switches are used.
Off: When the OFFSET/GAIN switch is in the SET position.</td></tr>
<tr><td>LINK RUN</td><td>On:
Off:</td><td>Normal communication
Receive data error</td></tr>
<tr><td>LINK ERR</td><td>On:
Off:</td><td>Receive data error
Normal communication</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>Test mode terminals</td><td>Shorted when setting offset/gain.</td></tr>
<tr><td>7</td><td>Analog output HOLD/CLEAR setting terminals</td><td>(1) HOLD setting: Short the terminals.
(2) CLEAR setting: Open the terminals.</td></tr>
<tr><td>8</td><td>Terminal block for twisted pair cables and power supply cables</td><td> 
</td></tr>
<tr><td>9</td><td>Reset switch</td><td>Hardware reset
Used to initialize buffer memory and operation processing of the A64DAVC/DAIC.
By turning this ON, the control input signal X5 of the A64DAVC/DAIC turns ON.
(Device number of control I/O signals depends on station setting.)</td></tr>
</table>

Table 6.1 Names and Description of Parts

6.4 Station Setting

By setting the station number of the A64DAVC/DAIC, addresses of the batch refresh communication areas where control I/O signal information is stored and the range of use of the remote terminal communication data areas where command data and read/write data are stored are designated. Perform station setting considering the following.

POINT

Do not change station setting during communication in the MINI-S3 link. If changed, output or input error may occur.

(1) The range of station setting is 1 to (64—[number of occupied points of this module]+1).

(2) The range of communication with remote I/O modules and remote terminal modules is determined by the total number of remote stations (initial data ROM).
For example, when the total number of remote stations is 10, communication is executed with the remote I/O modules and remote terminal modules of which station numbers are between 1 and 10.

(3) Station numbers can be set without regard to the order of connection of modules.
For example, station setting shown in Fig. 6.1 is allowed.

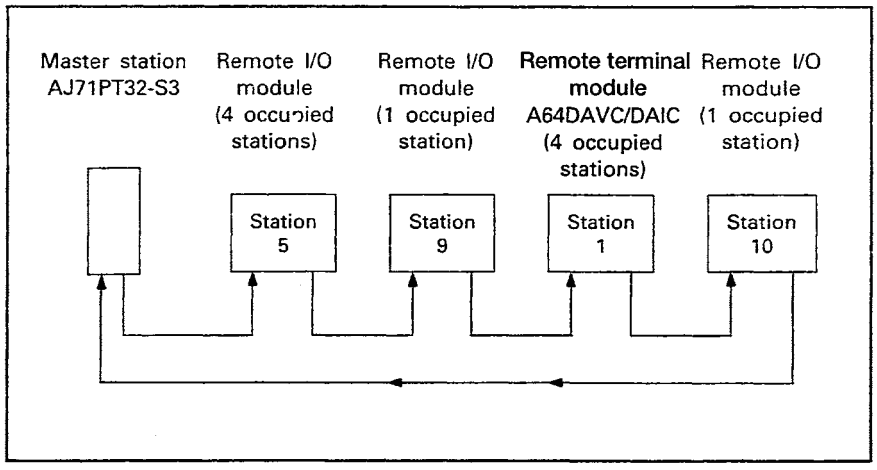


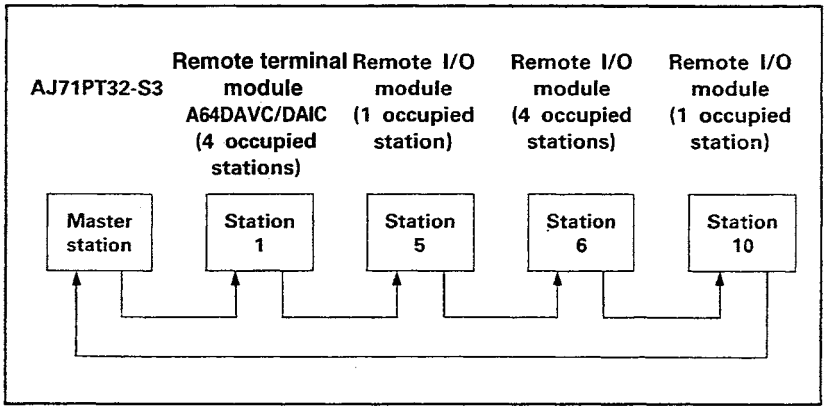
Fig. 6.1 Remote Module Station Setting

(4) Set station numbers not to leave unused stations (station numbers which correspond to no remote terminal module or remote I/O module).
f there is an unused station within the total number of remote stations (set with the initial data ROM), such station is detected as a communication error station.

POINT

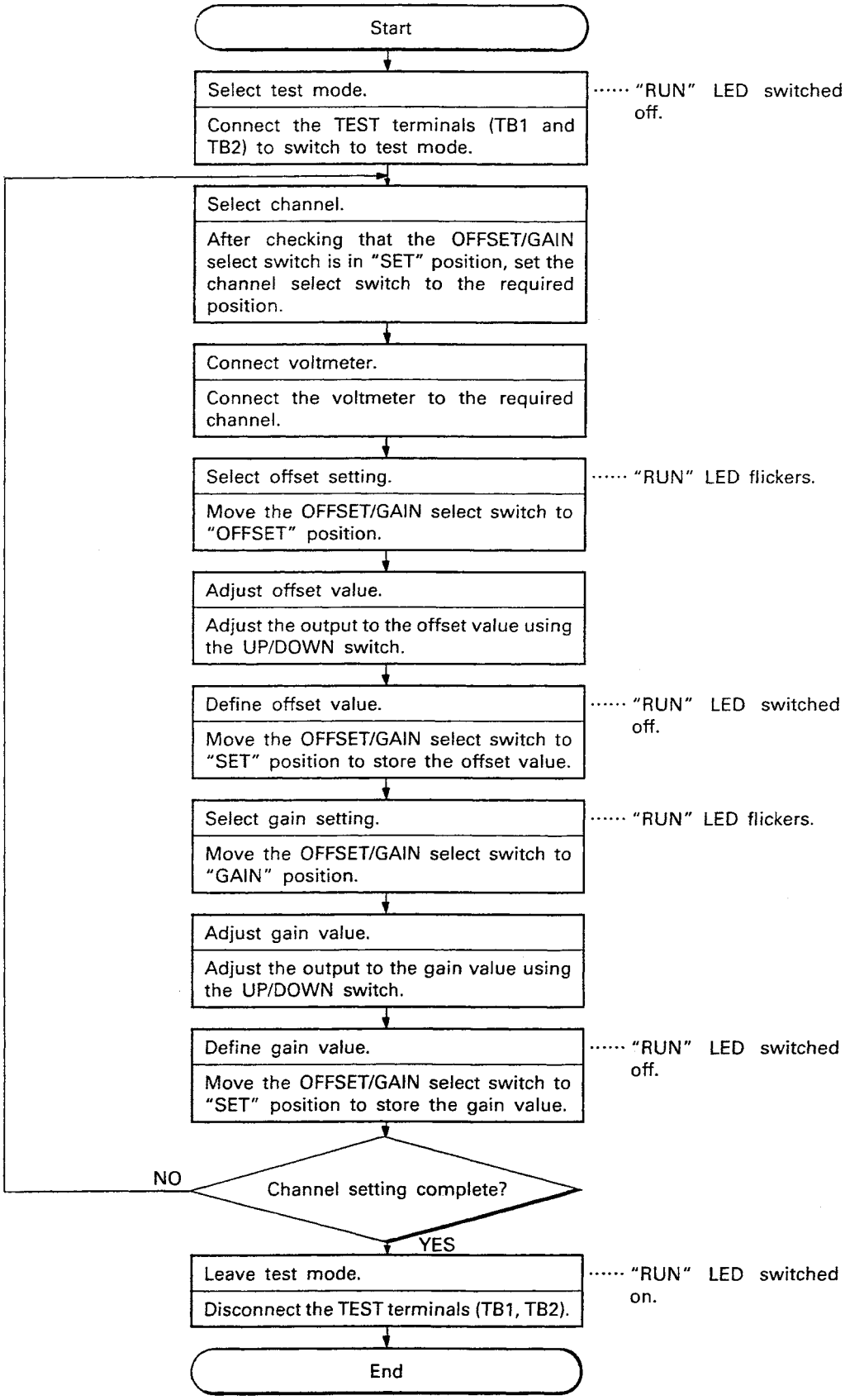
(1) Do not set any two or more stations for one same station number in the same loop. If two or more stations are set for the same station number, such stations may not operate normally. Make sure that there are no stations assigned with the same station number.

(2) If remote terminal or I/O modules which have two or more occupied stations are used, set station numbers skipping the numbers used for occupied stations. For example, if the A64DAVC/DAIC which has four occupied stations is set for station 1, shown below, do not set other remote I/O modules for stations 2, 3 and 4.



6.5 Offset/gain Setting Procedure

Follow the procedure flow shown below for offset/gain setting.



POINT

(1) The offset value and gain value are stored in the A64DAVC/DAIC and are not erased if the power is turned off.

(2) Do not select test mode during execution of D/A conversion.
Selecting test mode stops D/A conversion of all channels and affects control of external devices.

(3) Offset/gain setting is allowed within the following ranges:
• A64DAVC ····· −10 V to 0 V to 10 V
• A64DAIC ····· 0 mA to 40 mA
If any value set is outside the above range, overall accuracy may not be within the range of performance specifications.

(4) Before switching from one channel to another in test mode, the OFFSET/GAIN select switch should be set to the "SET" position.
If the channel is switched with the OFFSET/GAIN select switch in the "OFFSET" or "GAIN" position, the offset/gain value of the previous channel remains unchanged and the set value is stored to the new channel when the switch is set to "SET".

(5) The "RUN" LED flickers fast at intervals of 0.1 seconds to indicate that the offset/gain value specified has exceeded the allowed range.
When the "RUN" LED is flickering fast, the offset/gain value remains unchanged if the OFFSET/GAIN select switch is set to "SET".

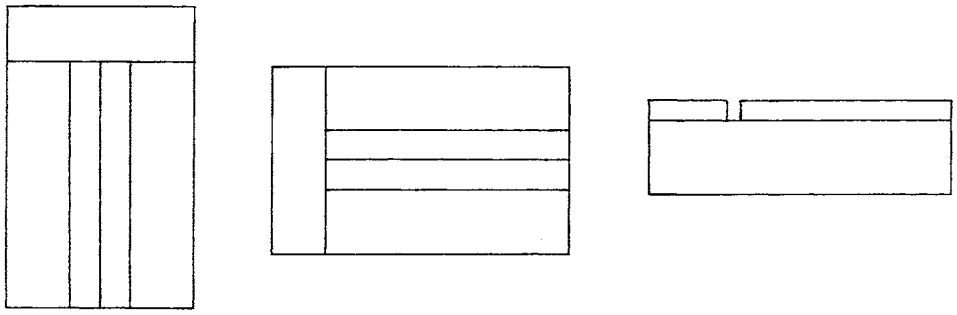
6.6 Analog Output HOLD/CLEAR Setting

HOLD/CLEAR of analog output when the PC CPU is stopped or the analog output enable signal is turned OFF is set with the HOLD/CLEAR terminals on the terminal block.
HOLD setting: Short the HOLD-CLEAR terminals.
CLEAR setting: Open the HOLD-CLEAR terminals.

6.7 Mounting Directions

(1) The A64DAVC/DAIC can be mounted in any direction (Front side must not face downward.)

(2) Examples



Upright Horizontal Front side up

6.8 Mounting to the DIN Rail

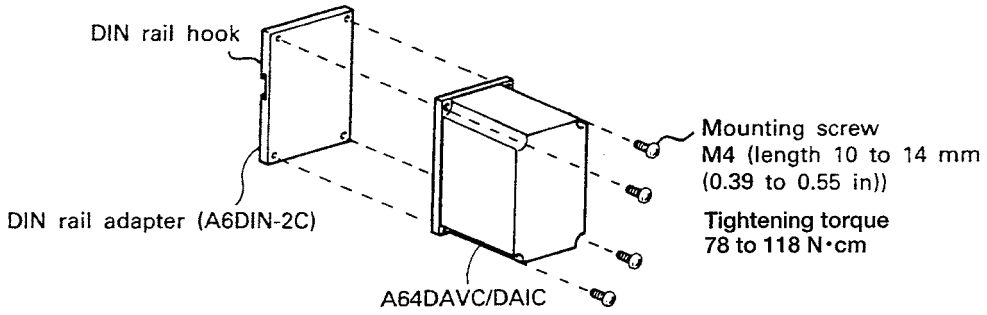
6.8.1 Fixing a DIN rail adapter to a module

(1) Specifications
Table shows specifications of the DIN rail adapters.

Item \ Type	A6DIN2C
Applicable module	A64DAVC/DAIC, special function module for others and A2C CPU
External dimensions mm (in)	106 (4.18) X 174 (6.85)
Weight kg	0.06

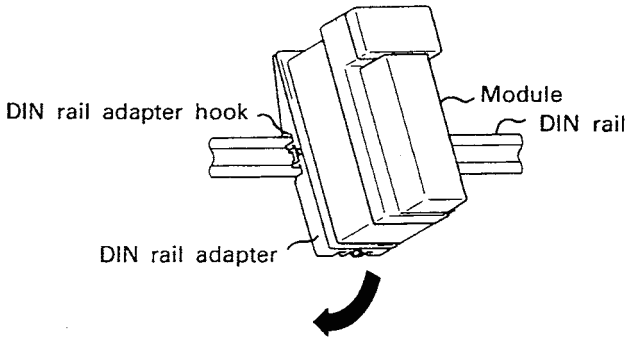
(2) Handling instructions
- Do not drop or give hard shocks to the DIN rail adapter since it is made of plastic.
- Use M4 screws of 10 mm (0.39 in) to 14 mm (0.55 in) long to fix a DIN rail adapter to a module. Torque range should be 78 to 118 N-cm.

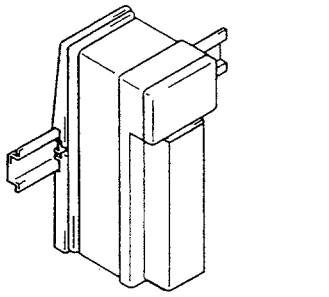
6.8.2 Fixing a DIN rail adapter to a module



6.8.3 Mounting to the DIN rail

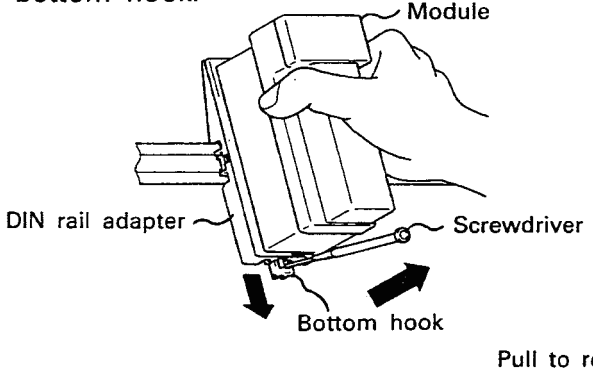
(1) Mounting procedure
After fixing the DIN rail adapter to the module, mount the module to the DIN rail as follows.
a) Engage the hook of the adapter with the rail from above the rail.
b) Push the module onto the rail and fix it in position.




A module mounted to DIN rail

c) When two adapters with module are mounted to the rail side by side without leaving a clearance between them, a 4 mm clearance is allowed between the modules.

(2) Removing procedure
Remove the module from the DIN rail as follows.
a) Pull down the bottom hook of the adapter using a screwdriver.
b) Pull the module away from the rail while pulling down the bottom hook.



Pull to remove.

6.9 Wiring of Data Link Cables

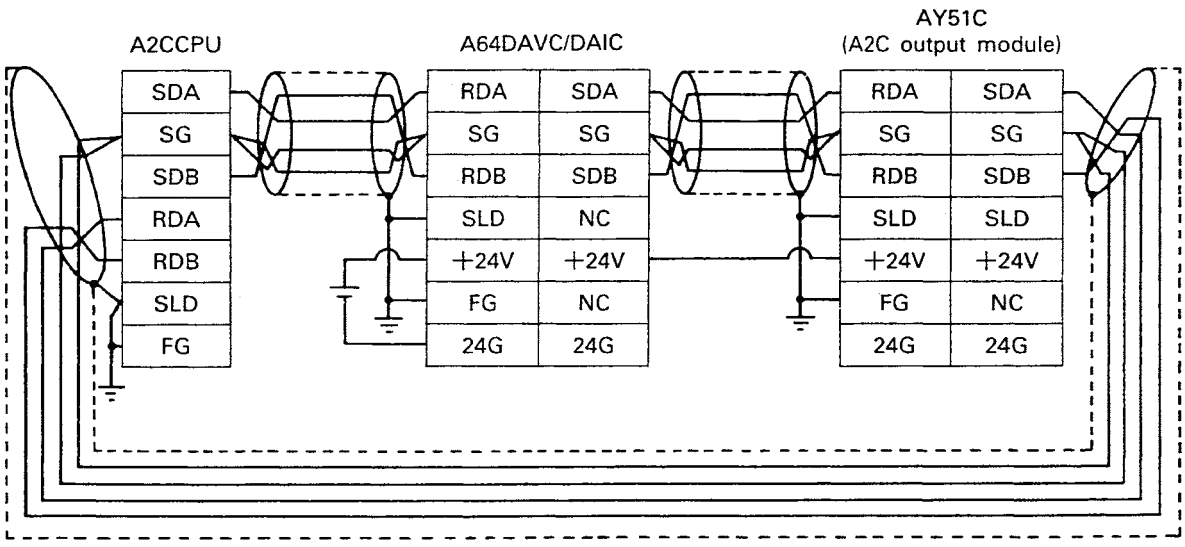
6.9.1 Handling instructions for twisted pair cables

Handle cables with special care.

(1) Do not compress the cable with rigid and sharp-edged material.
(2) Do not twist the cable extremely.
(3) Do not tense strong the cable.
(4) Do not step on the cable.
(5) Do not put things on the cable.
(6) Do not damage the insulation of the cable.

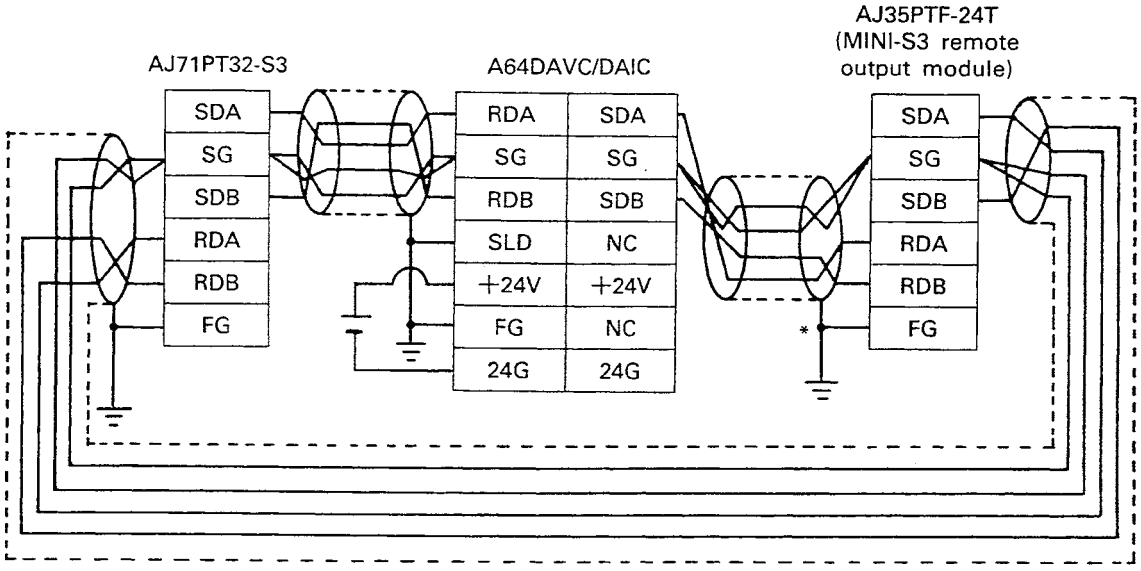
6.9.2 Connection of twisted pair cables

(1) Connecting the A2CCPU and the A64DAVC/DAIC



* Ground the shields at one point.

(2) Connecting the AJ71PT32-S3 and the A64DAVC/DAIC



* Ground the shields at one point.

The twisted pair shield cable terminal block uses the terminal screws shown below. Use appropriate solderless terminals.

Module Type	Terminal Screw	Tightening Torque Range N·cm
A2CCPU A64DAVC/DAIC A2C I/O module	M3.5	59 to 88
MELSECNET/MINI-S3 remote I/O module (batch refresh type)	M4	98 to 137

POINT

Twisted pair cables must be connected so that they may not be influenced by noise or serge induction.

(1) Do not lay the cables close to nor bind them together with main circuit wires, high-tension wires or load carrying wires. (allow 100 mm or more clearance)

(2) When connecting to the remote module terminal block, allow maximum clearance between twisted pair cables and module power supply lines and I/O signal wires.

(3) Do not use a part of twisted pair cables (such as one pair among 3 pairs) for power supply.

6.10 Wiring of Analog Input Signal Cable

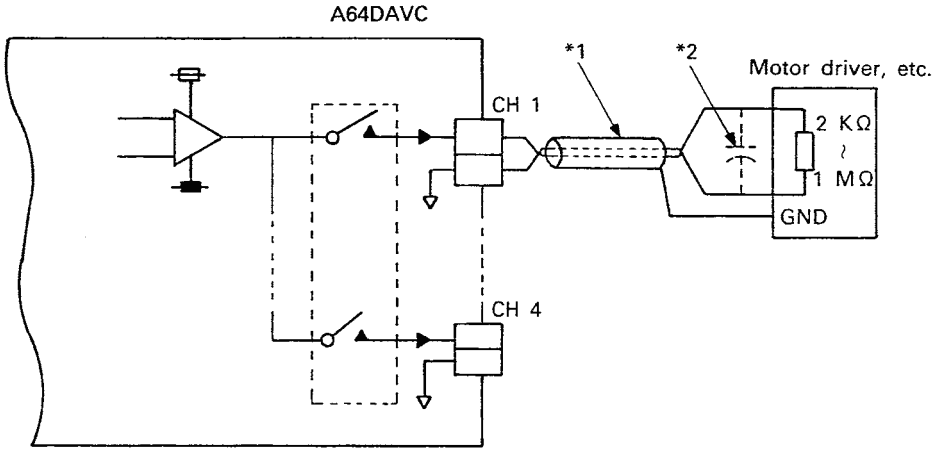
6.10.1 Wiring instructions

Protect external wiring against noise with the following precautions:

(1) Separate AC and DC wiring.
(2) Separate main circuit and/or high voltage wiring from control and signal wiring.
(3) Where applicable, ground the shielding of all wires to a common ground point.

6.10.2 Connection of the A64DAVC/DAIC to external devices

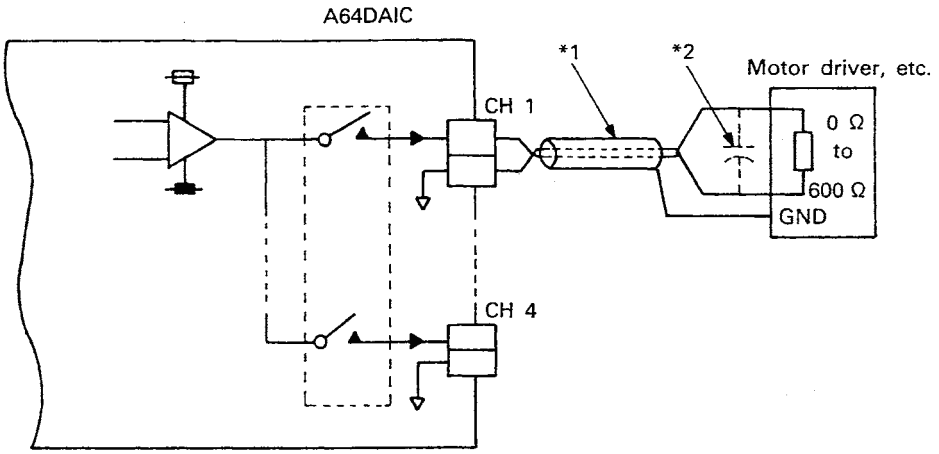
(1) Connection of the A64DAVC



Point

(1) Use two-core shielded wiring (twisted).
(2) If noise or ripple is generated by the external wiring, connect a 0.1 to 0.47 μF (25V or more voltage resistance parts) capacitor to the input terminal of the external device.

(2) Connection of the A64DAIC



Point

(1) Use two-core shielded wiring (twisted).
(2) If noise or ripple is generated by the external wiring, connect a 0.1 to 0.47 μF (25V or more voltage resistance parts) capacitor to the input terminal of the external device.

7. TROUBLESHOOTING

7.1 List of Error Codes

(1) If an error has occurred when data is written to the A64DAVC/DAIC (the RUN LED flickers), any of the error codes mentioned in the list below is stored in buffer memory at address 9. When the A2CCPU is used, the same error code is stored also in special registers D9180 to D9193. When the AJ71PT32-S3 is used, the same error code is stored also in buffer memory at addresses 196 to 209.

Error Code	Cause	Corrective Action
100 (64_H)	(Read error) • Designated head address is out of buffer memory. • Designated range of read words includes addresses out of buffer memory.	Correct data which designates range out of buffer memory.
101 (65_H)	(Write error) • Designated head address is out of buffer memory. • Designated range of write words includes addresses out of buffer memory. • Write was attempted to read-only areas.	• Correct data which designates range out of buffer memory. • Correct data which designates range read-only areas.
102 (66_H)	Command code other than read (1) or write (2) is received.	May be influenced by noise. Take measures against noise.
103 (67_H)	Data was received immediately after read command (1).	
104 (68_H)	Read and write word length is set at "0".	
105 (69_H)	The number of words set by write command data differs from that of received data.	
11 ⬚	Digital values were set out of the specified range. ⬚ indicates the channel on which the error occurred.	Correct digital values into the specified range.
12 ⬚	Analog output enable/disable setting was done with other than 0 or 1. ⬚ indicates the channel on which the error occurred.	Correct analog output enable/disable setting to 1 (enable) or 0 (disable).
130	Digital value resolution was set with other than 1, 2 or 3.	Correct digital value resolution setting to 1 (1/4000), 2 (1/8000) or 3 (1/12000).

Table 7.1 List of Error Codes (Errors Detected by the A64DAVC/DAIC)

(a) If two or more errors occur continuously, the error code for the first error is stored, and following error codes are not stored.

(b) Error code reset is done by writing "0" to address 9 of buffer memory. (Figures other than 0 are ignored.)

(2) When the AJ71PT32-S3 is used, error codes for the errors occur during communication with remote terminal modules are stored in buffer memory at addresses 196 to 209 in addition to the error codes for errors detected by the A64DAVC/DAIC (Table 7.1).

Error Code	Error Name	Cause	Corrective Action
1	Set data error	Data written to the remote terminal transmission areas includes errors.	Correct the data.
6	WDT error	Remote terminal module malfunction.	• Reset faulty remote terminal module. • Turn OFF and then ON the power. • If the above procedures do not recover the system, the system hardware is faulty. Please consult Mitsubishi representative.
8	Transmission area setting error	Remote terminal transmission area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.
9	Communication error	Communication between the master module and remote terminal modules is faulty.	Noise or remote terminal module failure.
11 (B_H)			
10 (A_H)	Receive area setting error	Remote terminal receive area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.

Table 7.2 List of Error Codes (Errors Detected by the AJ71PT32-S3)

7.2 When the RUN LED Flickers or Turned OFF

(1) When flickers:

Check Point	Corrective Action
Data which disables write or read is written to the A64DAVC/DAIC.	• Refer to the List of Error Codes (Section 7.1) for the cause, and correct the sequence program. • Check the transmission system and influence of noise.
The TEST terminals are shorted. (Test mode)	Perform offset/gain adjustment, and then, open the TEST terminals.
The LED is flickering at 0.1 sec intervals in test mode.	Perform offset/gain adjustment in the specified range.

(2) When turned OFF:

Check Point	Corrective Action
24 VDC power supply is turned on.	Make sure the power supply.
24 VDC power supply voltage is within the set range.	Adjust the voltage within 15.6 to 31.2 V range.
If the MINI-S3 link is connected, the MINI-S3 link communication start signal Y(n+28) is turned ON.	Add a loop to turn ON the MINI-S3 link communication start signal Y(n+28) to the sequence program.
If the MINI-S3 link is connected, error code "6" may be stored in the master module buffer memory at address 196 to 209.	Reset the PLC CPU, and start them in the same manner. If error code "6" is again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
If the MINI-S3 link is connected, error codes "9" and "10" may be stored in the master module buffer memory at address 196 to 209.	Reset the PLC CPU, and start them in the same manner. If error codes "9" and "10" are again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
Data link cables are normal.	Check the cables referring to Section 6.9.
The TEST terminals are shorted. (Test mode)	After offset/gain setting, open the TEST terminals.

7.3 When the LINK RUN LED Turned OFF or the LINK ERR. LED Turned ON

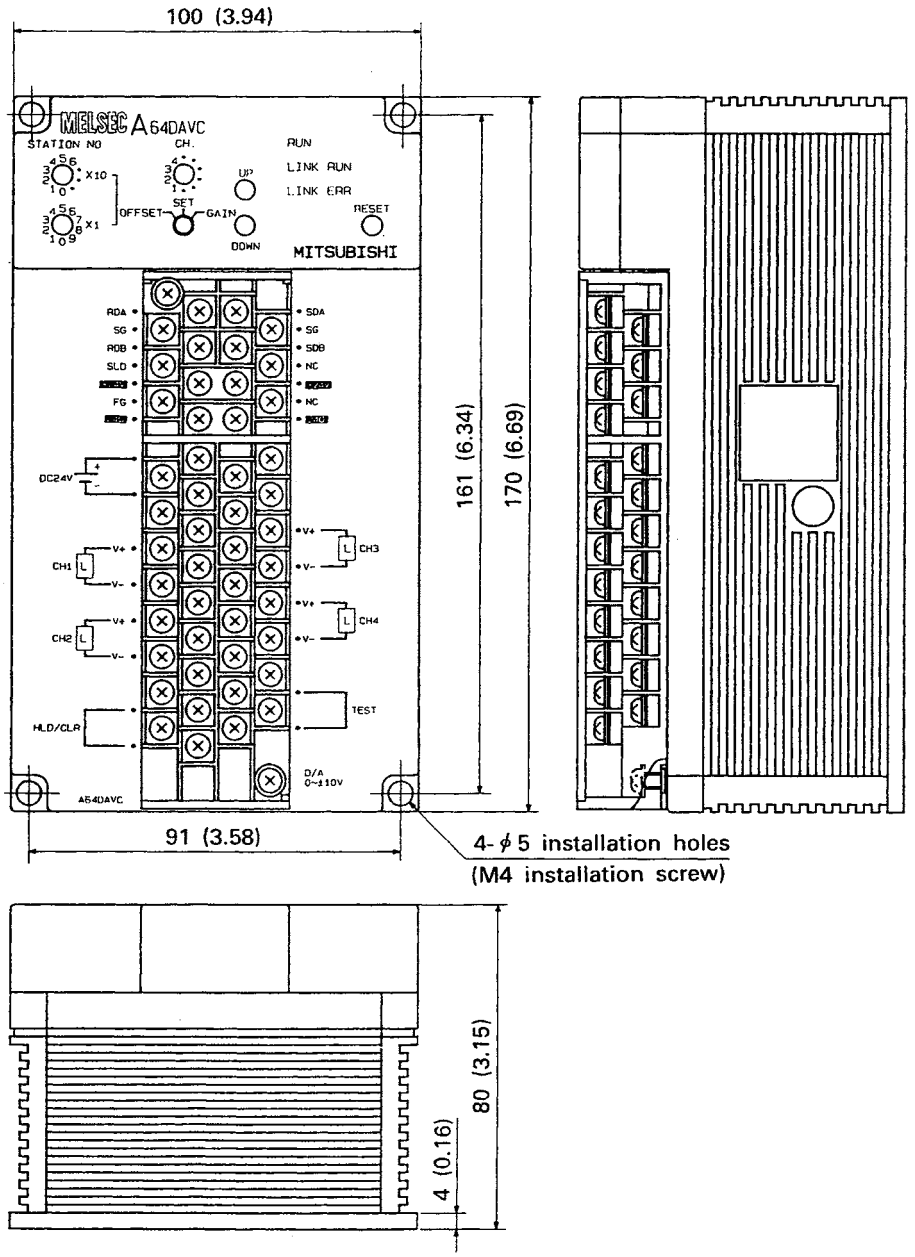
Check Point	Corrective Action
The RUN LED is flickering.	Follow Section 7.2 (1).
The RUN LED turned OFF.	Follow Section 7.2 (2).

7.4 When Analog Output Is Not Provided Correctly

Check Point		Corrective Action
The RUN LED is flickering or turned OFF.		Follow Section 7.2.
The ERROR LED of the CPU module is flickering or turned ON.		Refer to the User's Manual for respective CPU module for error content.
The RUN LED of the CPU module is flickering or turned OFF.		Refer to the User's Manual for respective CPU module for error content.
When A2CCPU is used:	The RD/SD LED of the CPU module is flickering. (normal)	Refer to the A2CCPU User's Manual for error content.
When AJ71PT32-S3 is used:	The MINI-S3 link communication start signal Y(n+28) is turned ON.	Set the sequence program to turn ON the MINI-S3 link communication start signal.
	The RUN LED of the master module is turned OFF.	Refer to the AJ71PT32-S3 User's Manual for error content.
	The RD/SD LED of the master module is flickering. (normal)	Refer to the AJ71PT32-S3 User's Manual for error content.
Analog input signal lines are broken or disconnected. Locate trouble by checking the signal lines visually and for continuity. Disconnect the wiring from the analog output of the A64DAVC/DAIC and measure analog output at the module terminals.		• If analog output measured at the module terminals is correct, the external wiring may be broken or affected by noise. Check all wiring and grounding. • Separate the module from the frame and disconnect the grounding circuit. (Mount the module to the DIN rail.)

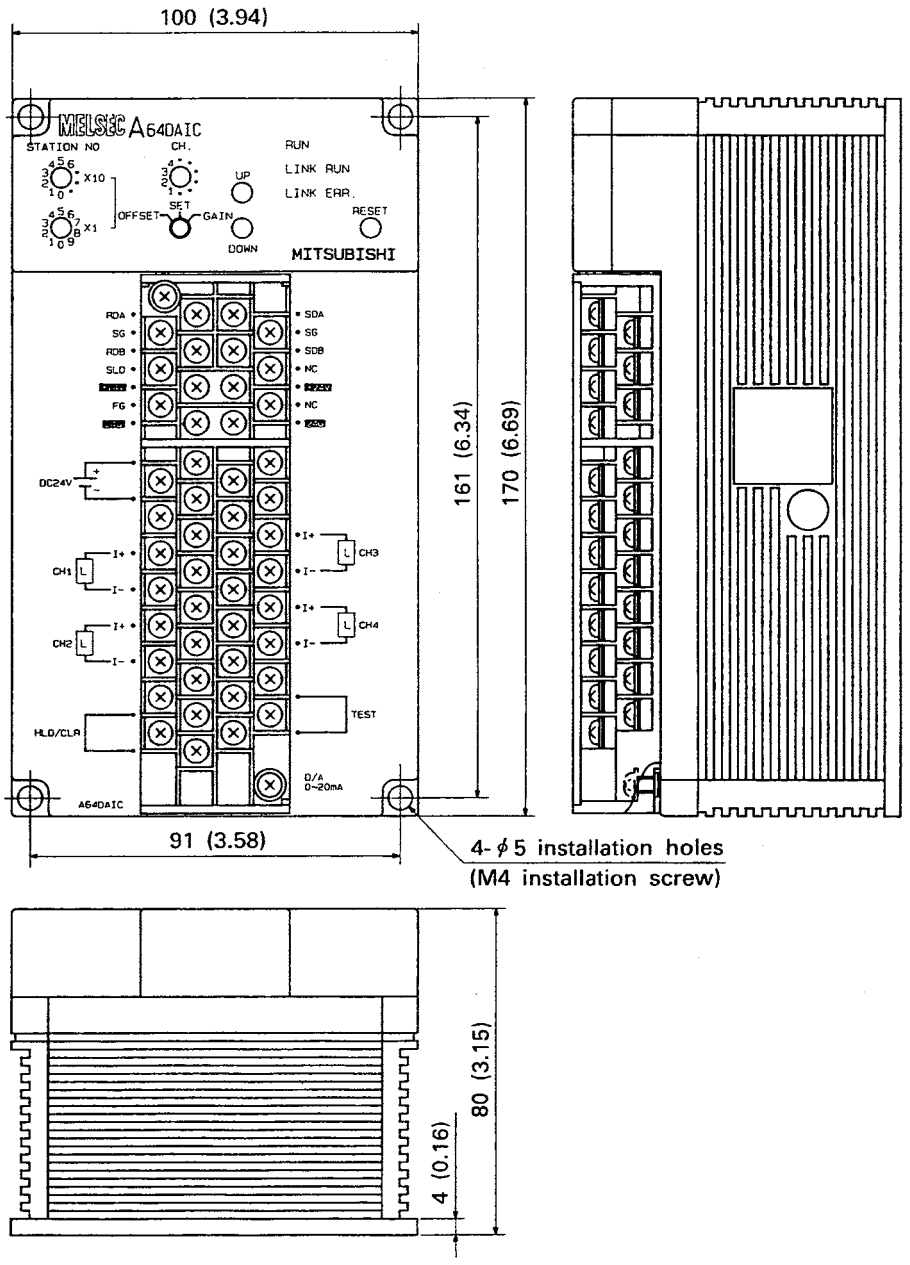
APPENDICES

Appendix 1 A64DAVC Outside Dimensions



Unit: mm (in)

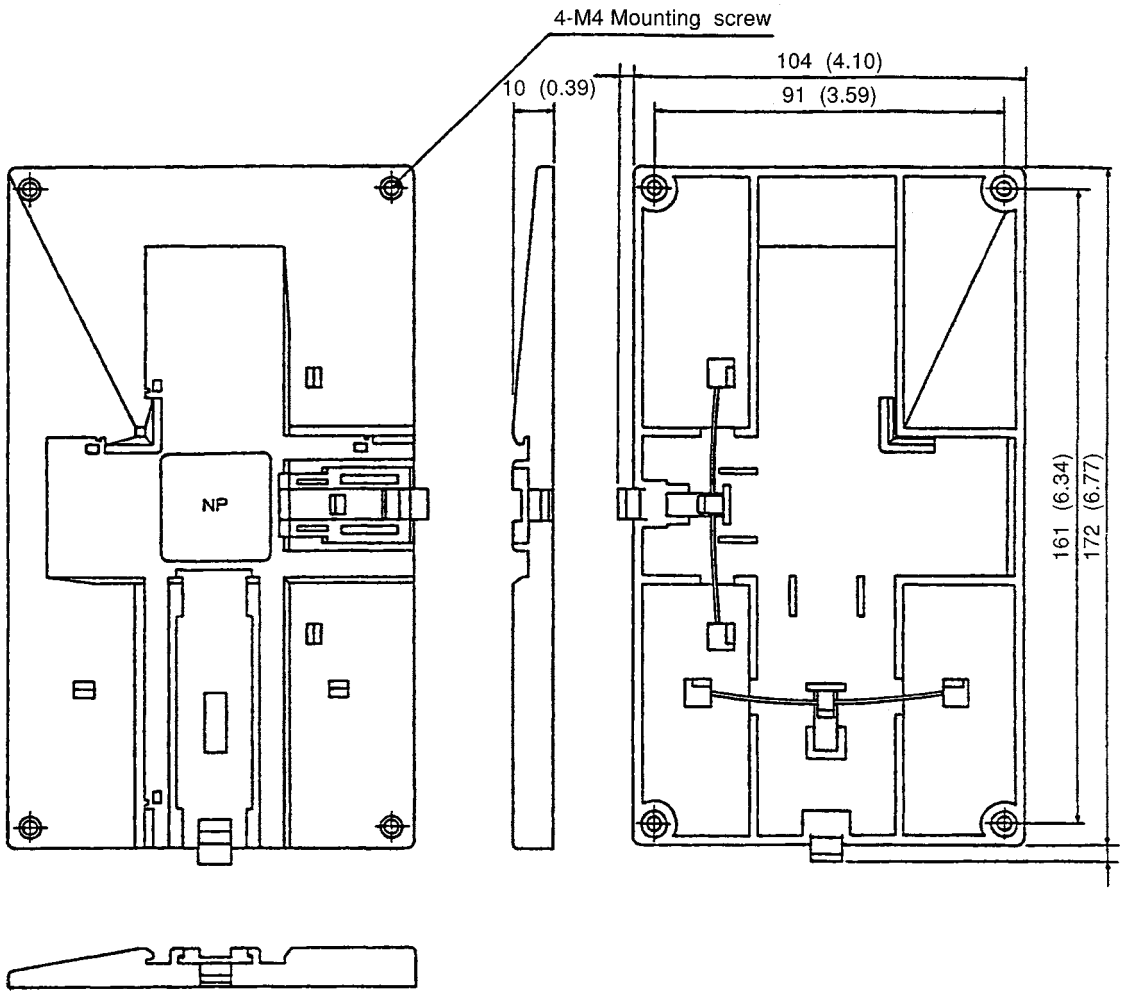
Appendix 2 A64DAIC Outside Dimensions



Unit: mm (in)

APP

Appendix 3 DIN Adapter Dimensions



Unit: mm (in)

MEMO

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.

However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.

Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.

(2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications.

In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications.

However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

Digital-Analog Converter Module Type A64DAVC/A64DAIC

User's Manual

MODEL	A64DAVC/DAIC-U-E
MODEL CODE	13J783
IB(NA)-66248-C(0603)MEE	

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